

Hellcat 15 Upsell Schematics

Tiger Lake - U/ LPPDR4X

2020-08-03

REV : A00

DY : None Installed

UMA: UMA only installed

OPS: DISCRTE OPTIMUS installed

<Core Design>



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Title

Cover Page

Size
A3

Document Number

Hellcat 15" Upsell TGL

Rev

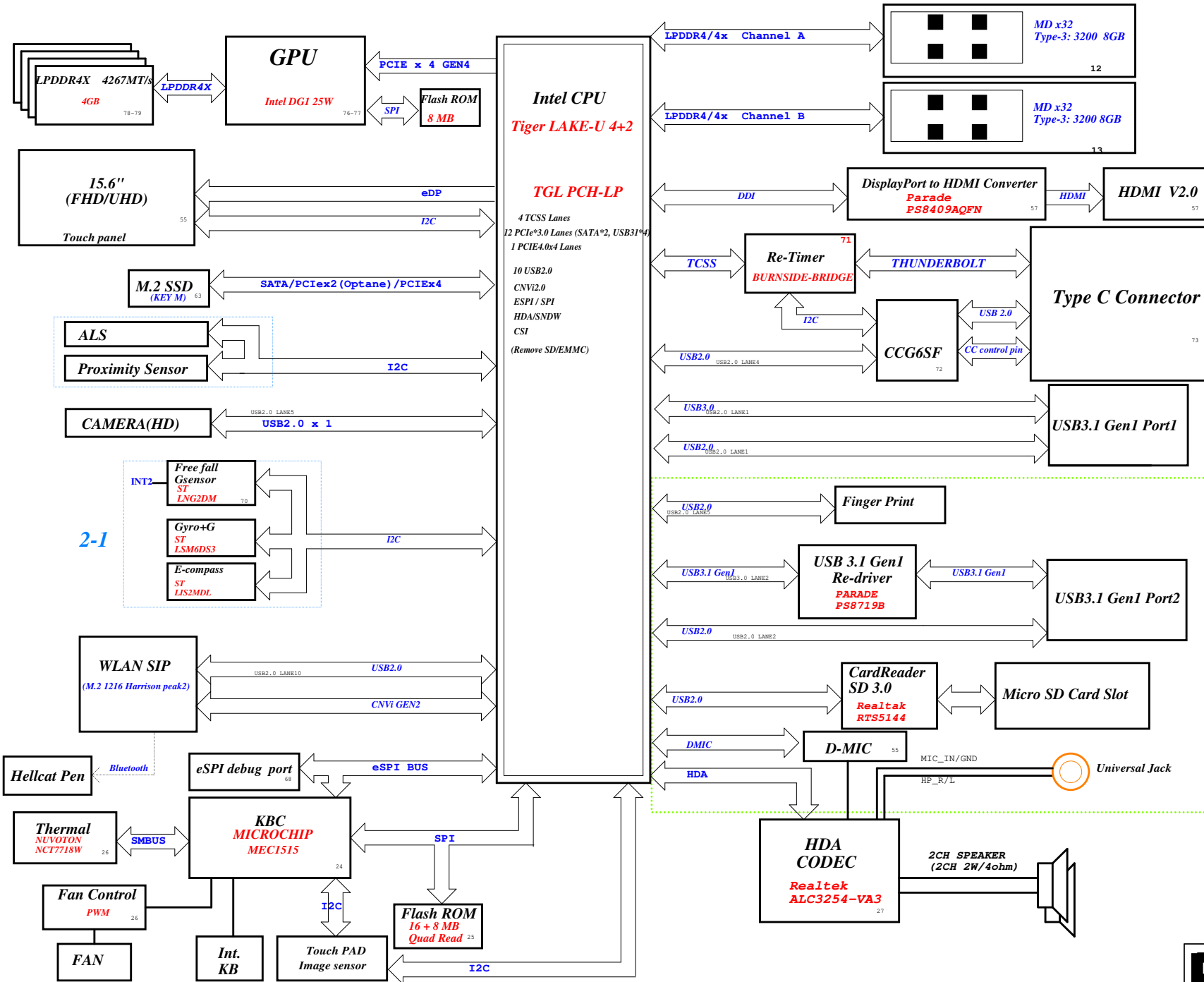
-1

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Hellcat 15 Upsell CPU 15W + GPU 25W Block Diagram

Project code: 4PD0HC010001
PCB P/N: 19828
Revision: X00 <https://vinafix.com>

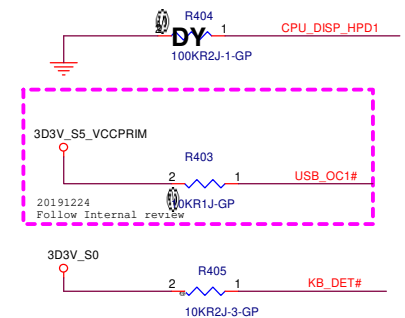


IO Board

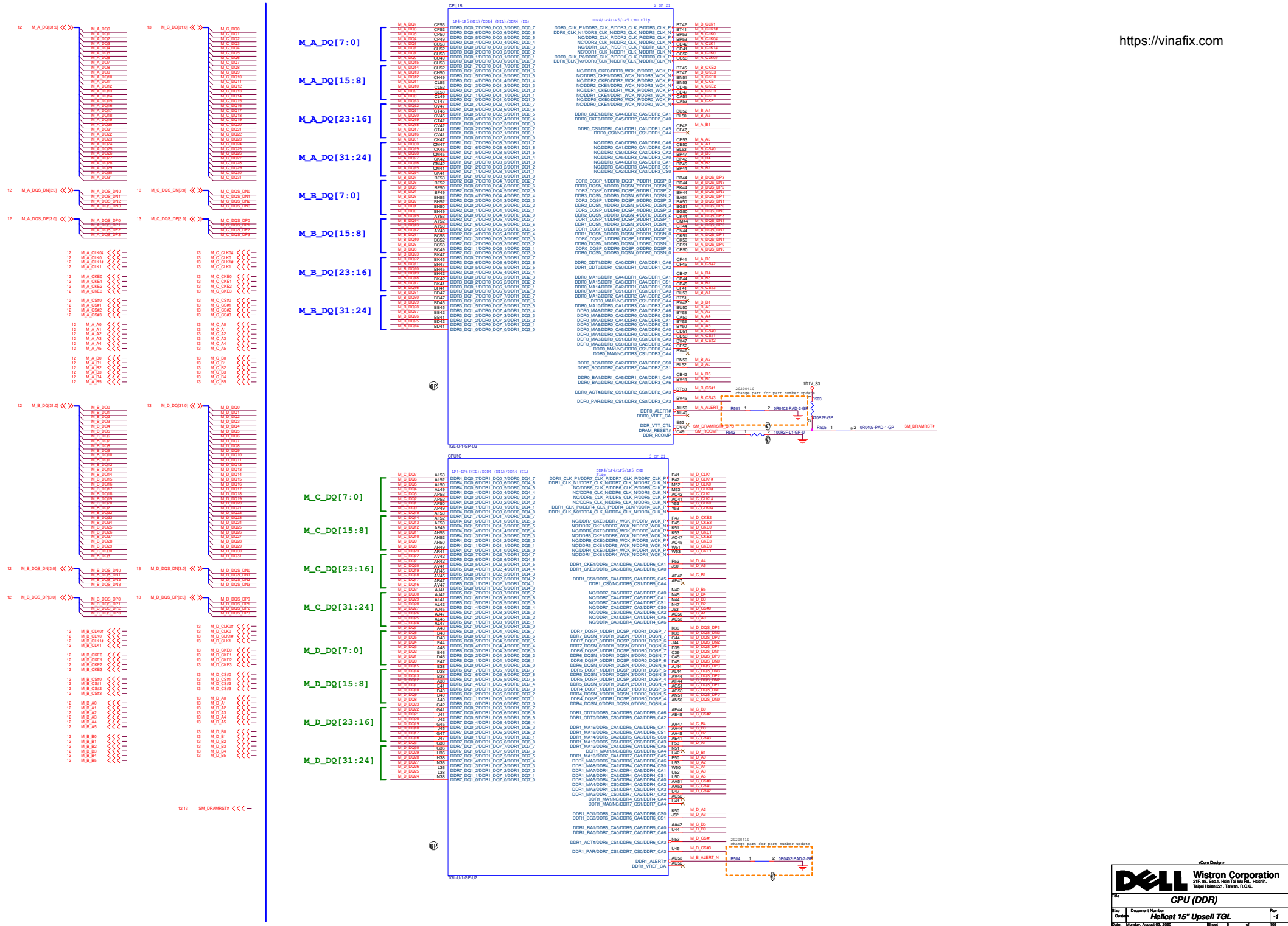
Title	CPU (DDI/EDP/TBT/TPC/)
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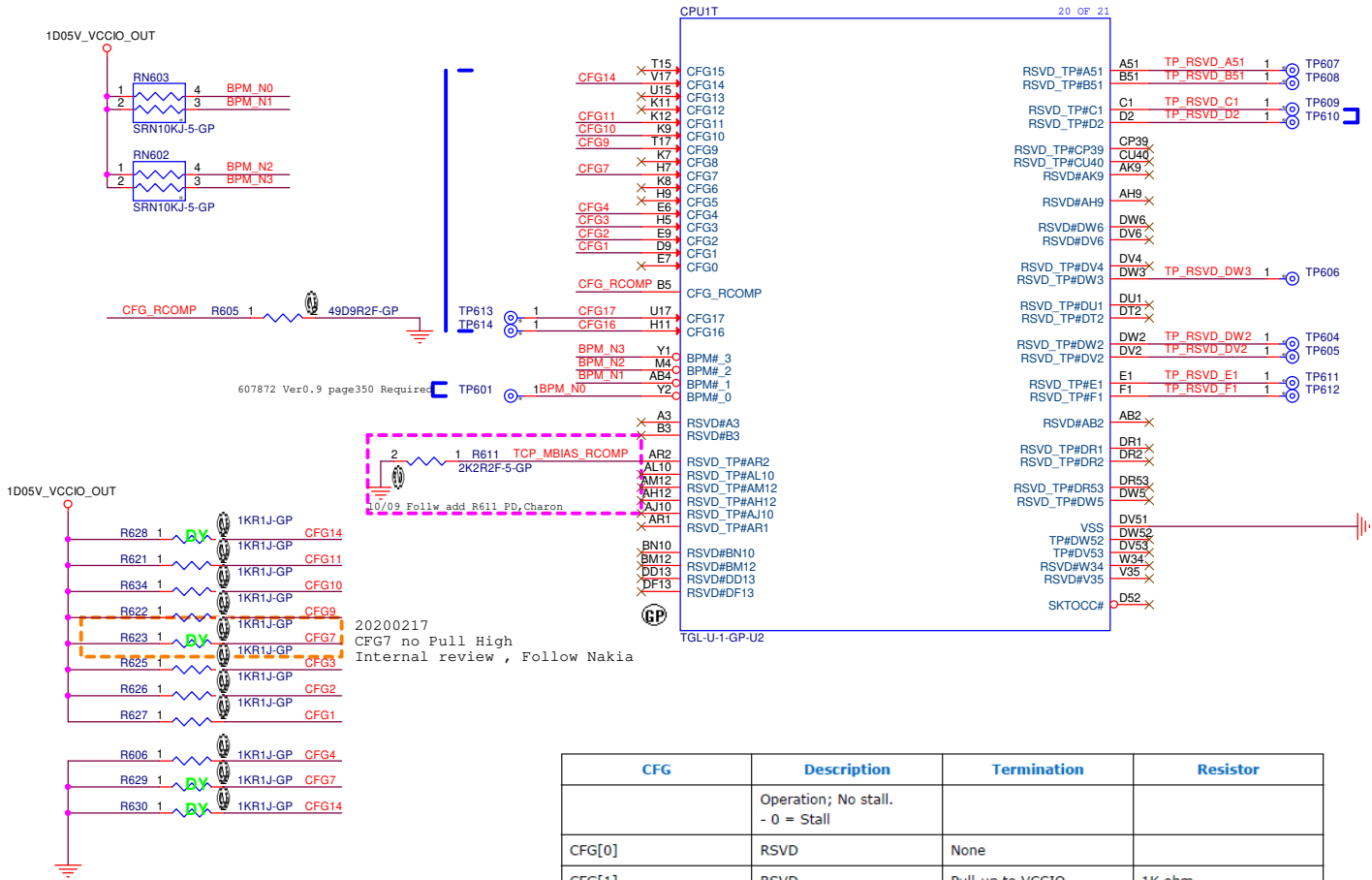


CFG1 >>>—
CFG2 >>>—
CFG3 >>>—
CFG4 >>>—

CFG7 >>>—
CFG9 >>>—
CFG10 >>>—
CFG11 >>>—

CFG14 >>>—
CFG16 >>>—
CFG17 >>>—

BPM_N0>>>—
BPM_N1>>>—



PCIEXPRESS STATIC LANE REVERSAL FOR ALL PEG PORTS	
CFG2	1: (DEFAULT)NORMAL OPERATION; 0:LANE REVERSAL
DISPLAY PORT PRESENCE STRAP	
CFG4	0: ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT 1: DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT
PCIE PORT BIFURCATION STRAPS	
CFG6[6:5]	11: DEVICE1 FUNTION 1, DEVICE 1 FUNCTION2 DISABLED 10: DEVICE1 FUNCTION1 ENABLED DEVICE1 FUNCTION 2 DISABLED 01: DEVICE 1 FUNCTION 1 DISABLED, DEVICE 1 FUNCTION 2 ENABLED 00: DEVICE 1 FUNCTION 1 ENABLED, DEVICE 1 FUNCTION 2 ENABLED

CFG	Description	Termination	Resistor
	Operation; No stall. - 0 = Stall		
CFG[0]	RSVD	None	
CFG[1]	RSVD	Pull-up to VCCIO	1K ohm
CFG[2]	RSVD	Pull-up to VCCIO	1K ohm
CFG[3]	RSVD	Pull-up to VCCIO	1K ohm
CFG[4]	eDP enable Strap: - 1 = Disabled. - 0 = Enabled.	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[6:5]	RSVD	None	
CFG[7]	PEG deferred link training	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[8]	RSVD	None	
CFG[11:9]	RSVD	Pull-up to VCCIO	1K ohm
CFG[13:12]	RSVD	None	
CFG[14]	PEG60 Lane Reversal: - 1 - (Default) Normal - 0 - Reversed	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[1 7:15]	RSVD	None	

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Title

CPU (CFG/IST)

Size A3

Document Number

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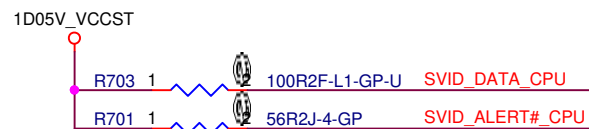
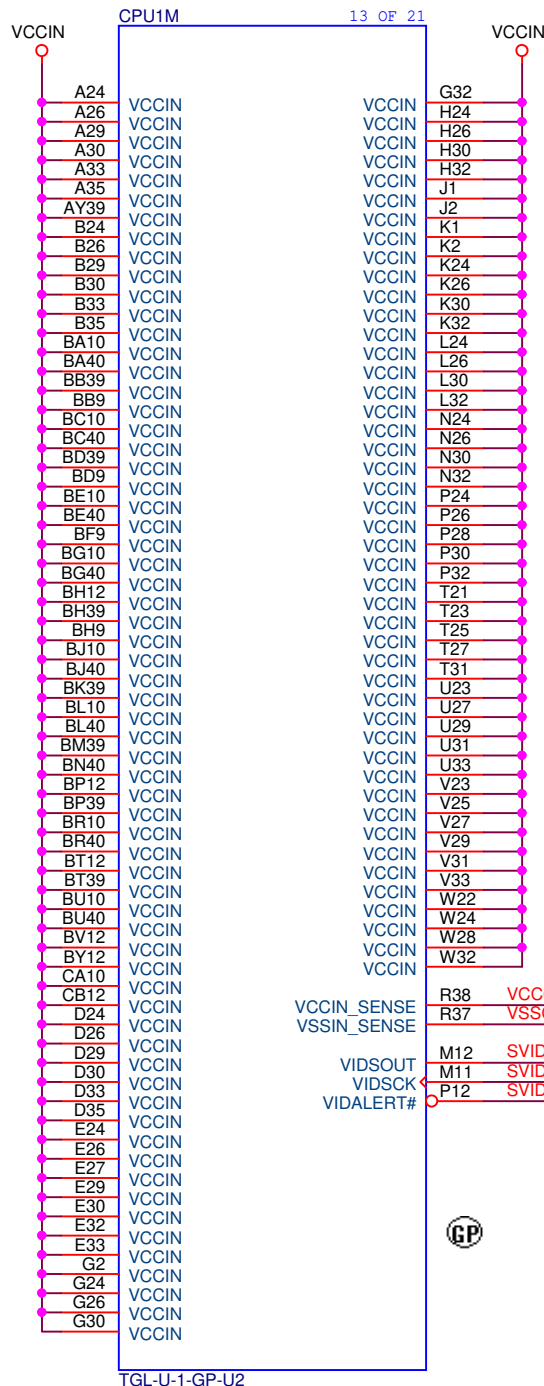
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46 VCCCORE_SENSE <<<—
46 VSSCORE_SENSE <<<—
46 SVID_ALERT#_CPU <<<—
46 SVID_CLK_CPU <<<—
46 SVID_DATA_CPU <<>>—

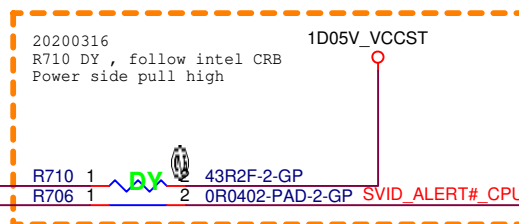
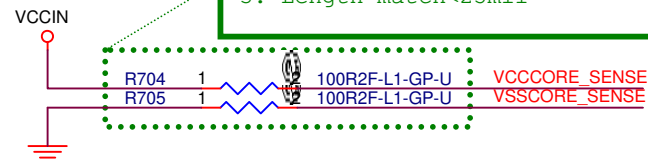
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Layout Note:
3.Length matchin 25mil, and close SOC in 2inch "

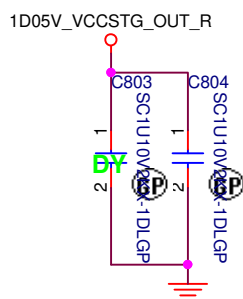
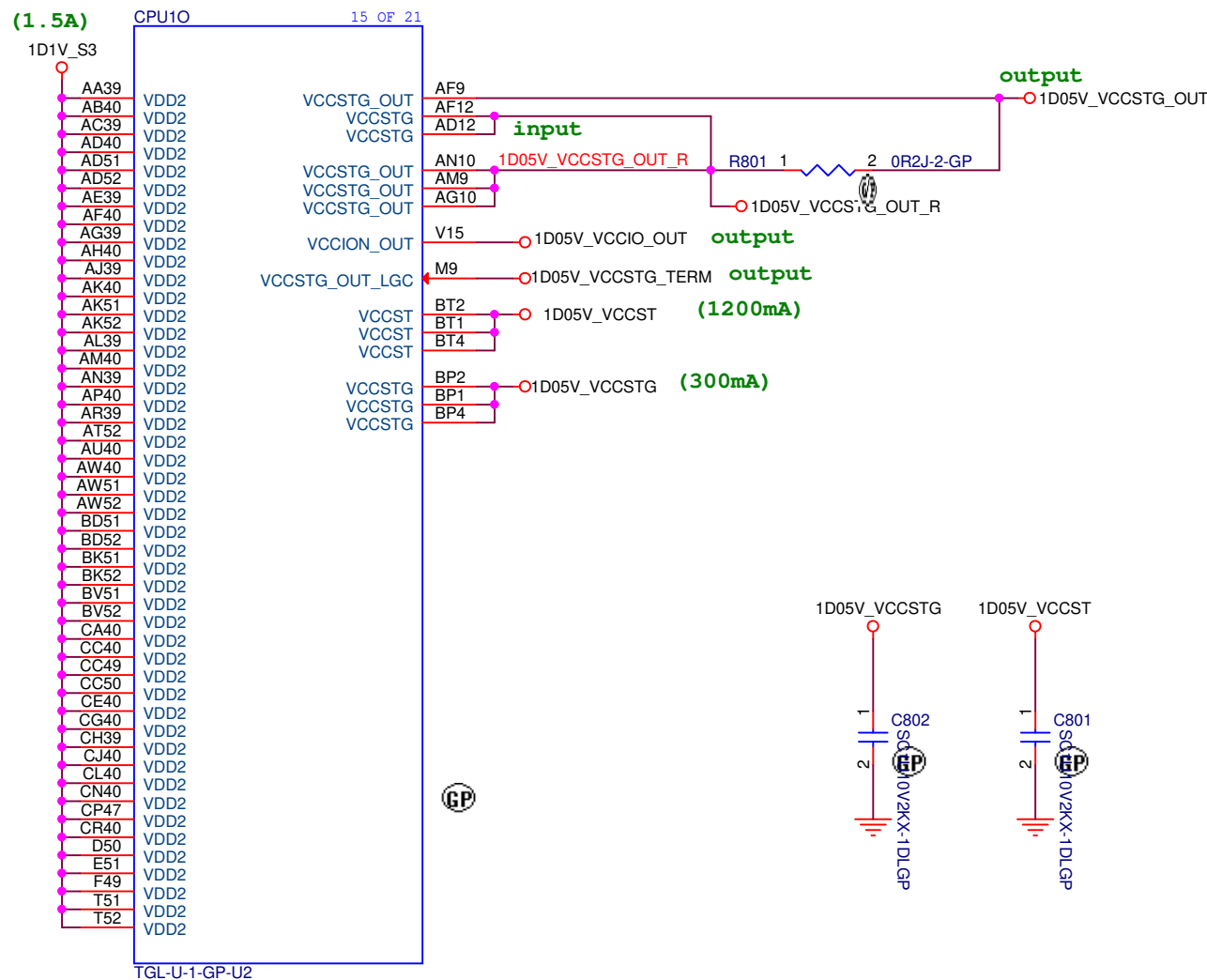
Layout Note:

1. Place close to CPU within 2"
2. VCC_SENSE/ VSS_SENSE
impedance=50 ohm
3. Length match<25mil

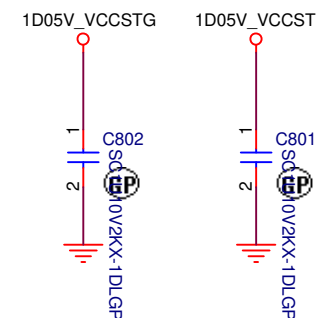


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Title CPU (VCCIN/VID)					
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C803 close to pin AN10, AM9
C804 close to pin AF12, AD12



Lack of VCCPLL_OC / VCC1P8A / VCCPLL

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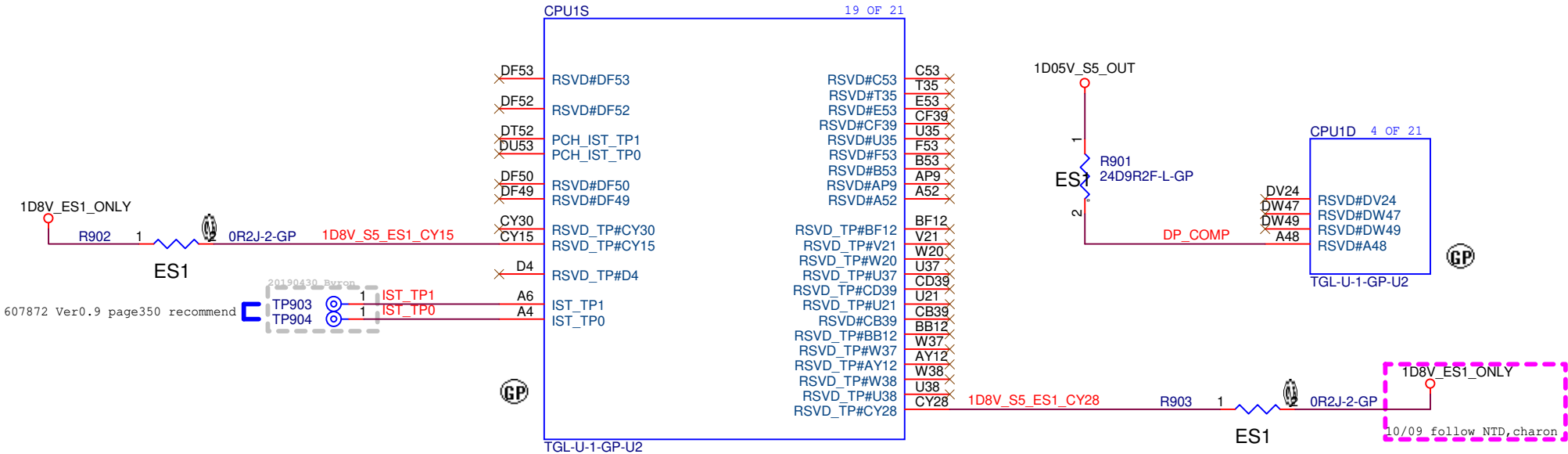
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Title **CPU (VDDQ/VCC/VCCST)**

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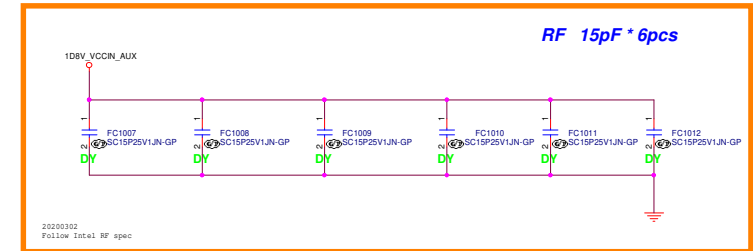
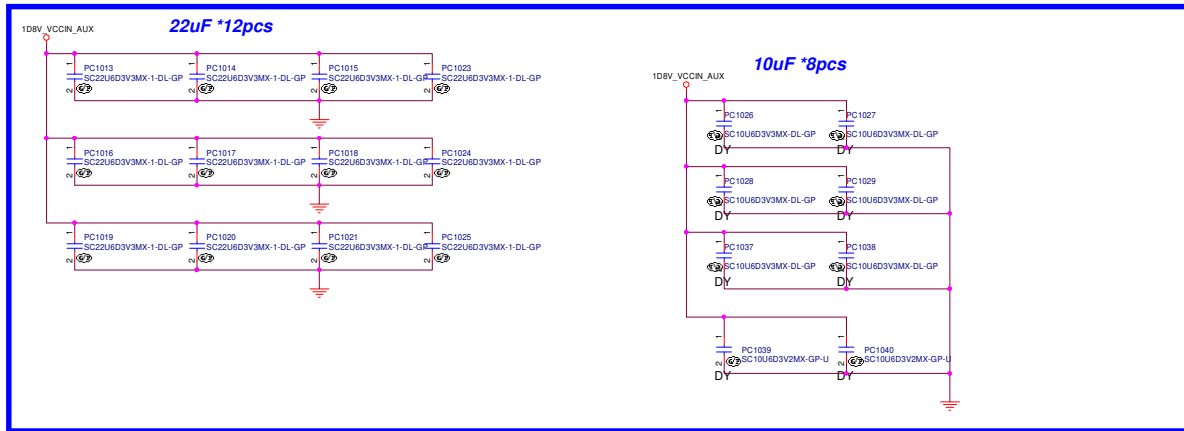
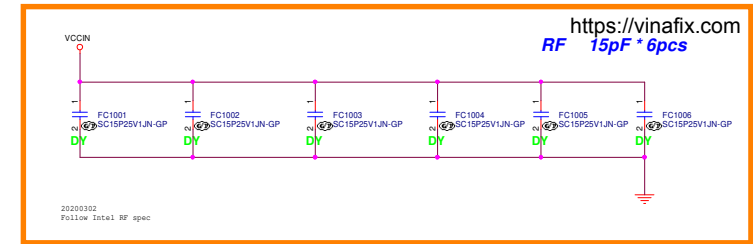
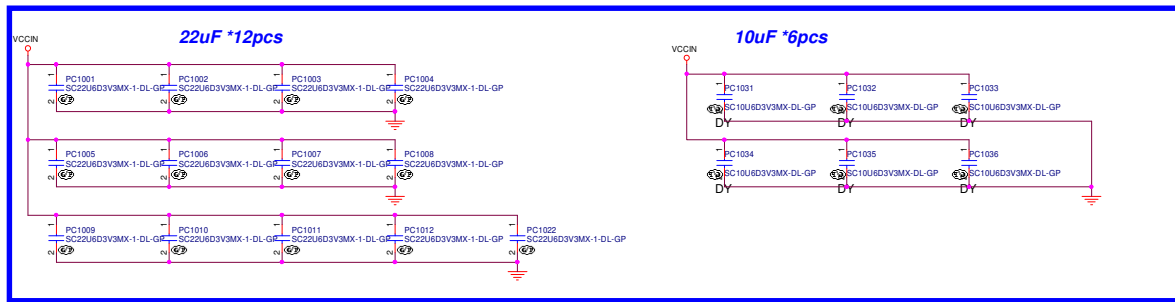
Title

CPU (RSVD)

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Main Func = CPU

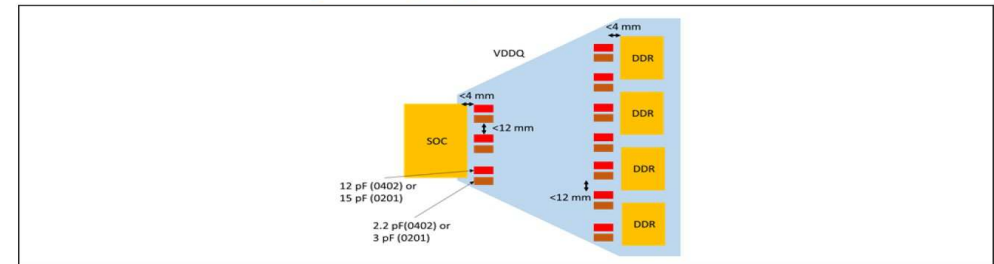


- In Intel validation, 6 x 0201 15 pF capacitors can achieve ~4 dB FIVR harmonic reduction based on Intel Ice Lake reference system validation.

Example: Placement of Caps in Intel Internal System

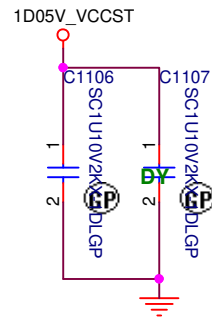
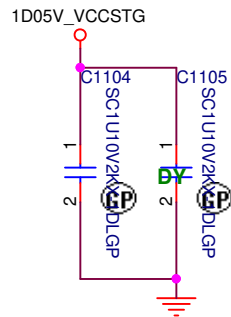
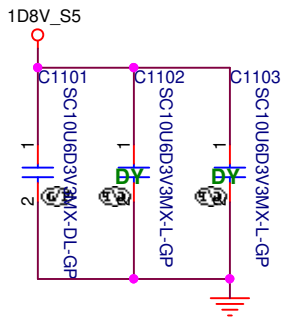
solid GND plane.

Figure 62. DDR Power Plane RF Cap Decoupling

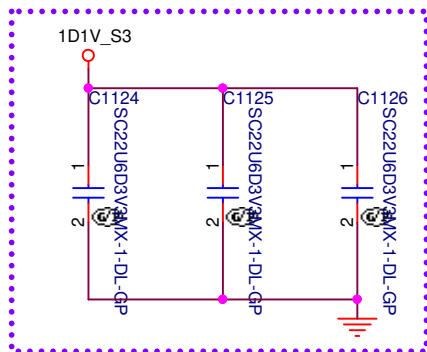


DRAM Devices:

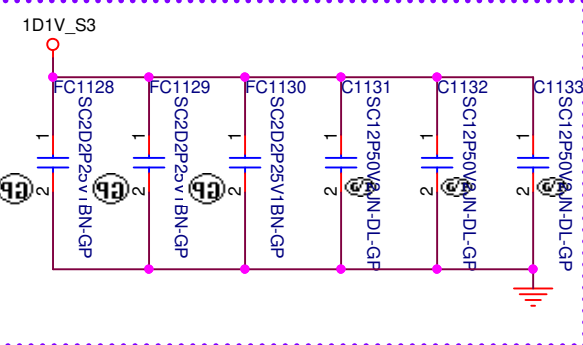
DRAM devices can radiate broadband and narrowband RFI noise and may cause radio



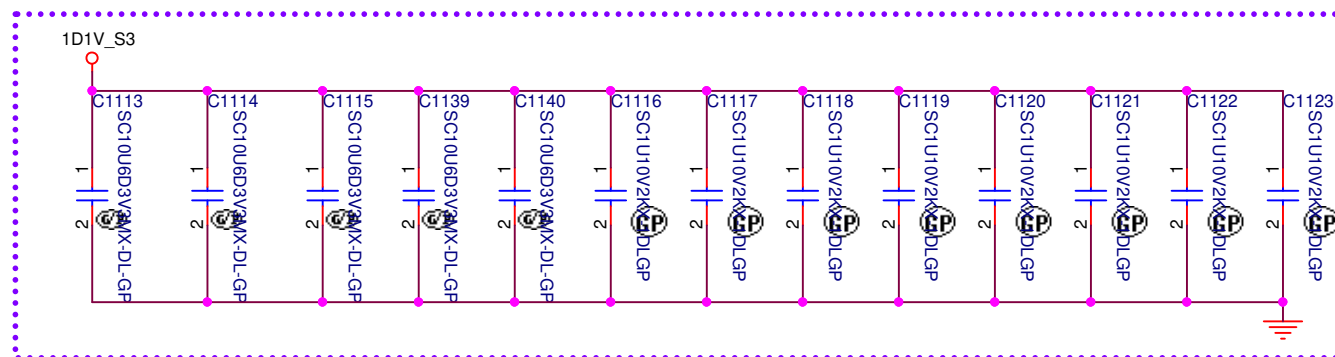
PLACE on CPU Same Side



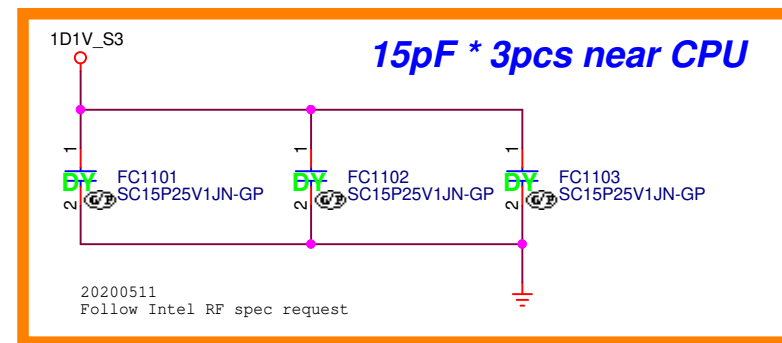
EMC CAPS - PLACE <4mm FROM SOC VDDQ,
WITH EACH PAIR <12mm APART




PLACE on BACK SIDE

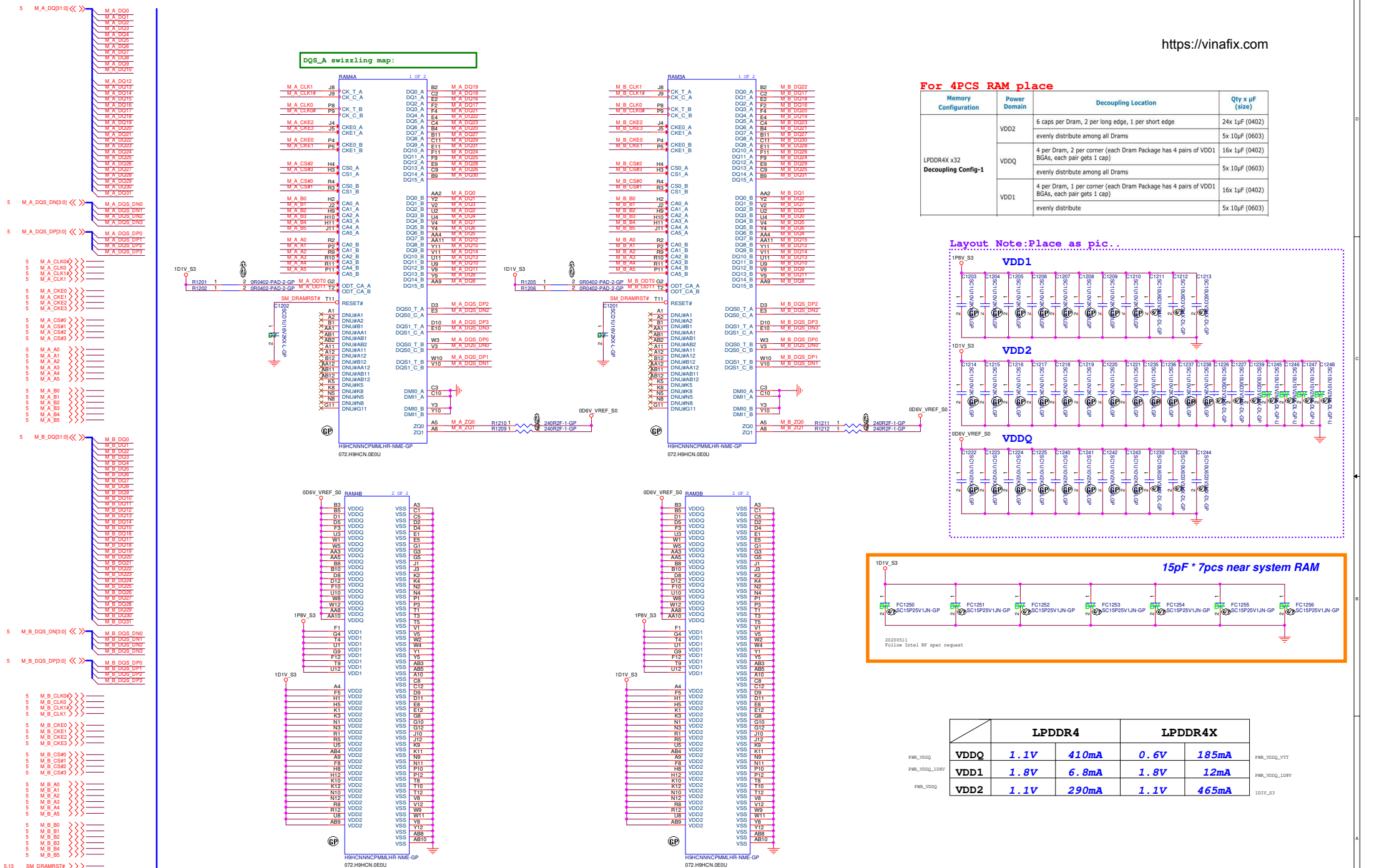


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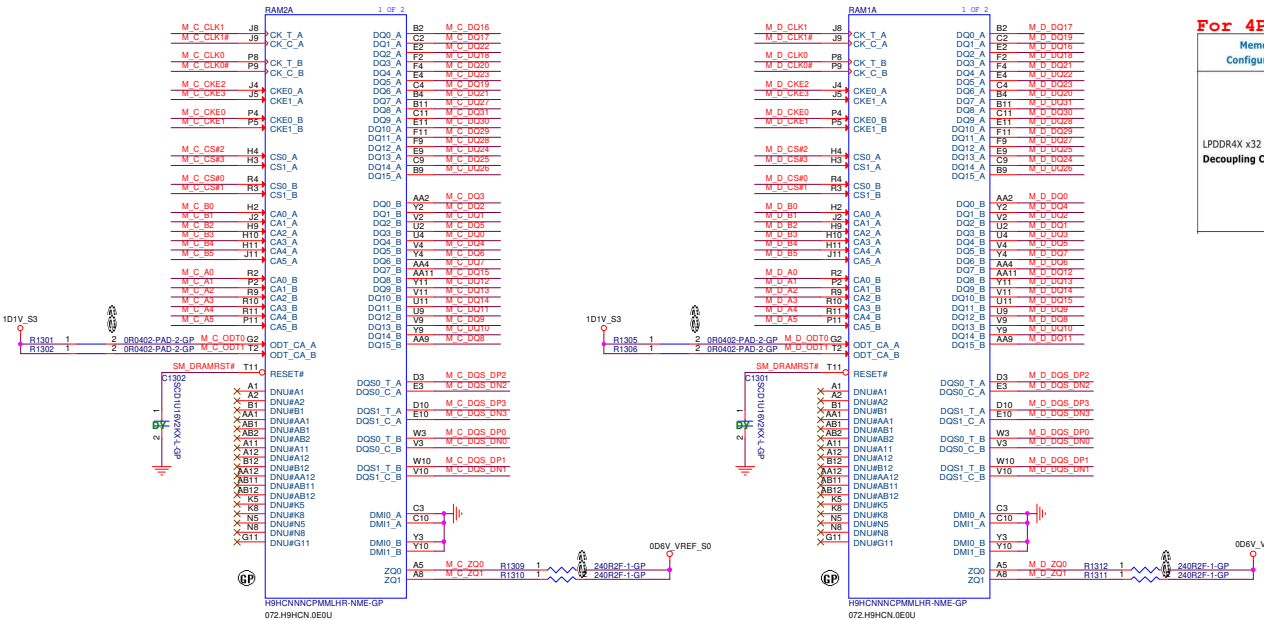


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Title CPU (Power Cap2)		
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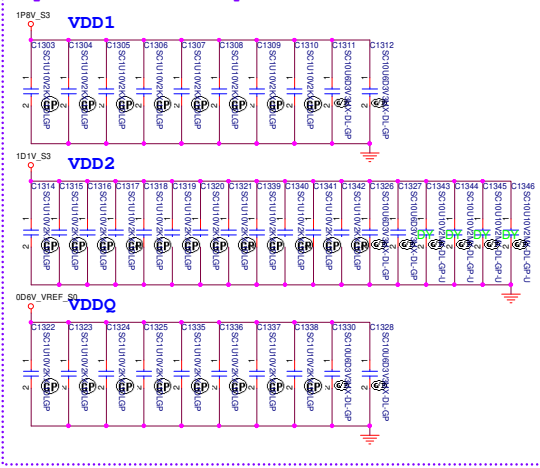
DQS_B swizzling map:



For 4PCS RAM place

Memory Configuration	Power Domain	Decoupling Location	Qty x μ F (size)
LPDDR4X x32 Decoupling Config-1	VDD2	6 caps per Dram, 2 per long edge, 1 per short edge evenly distribute among all Drams	24x 1 μ F (0402)
	VDDQ	4 per Dram, 2 per corner (each Dram Package has 4 pairs of VDD1 BGAs, each pair gets 1 cap) evenly distribute among all Drams	16x 1 μ F (0402) 5x 10 μ F (0603)
	VDD1	4 per Dram, 1 per corner (each Dram Package has 4 pairs of VDD1 BGAs, each pair gets 1 cap) evenly distribute	16x 1 μ F (0402) 5x 10 μ F (0603)

Layout Note: Place as pic..



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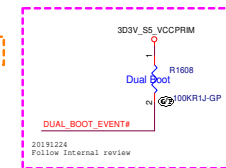
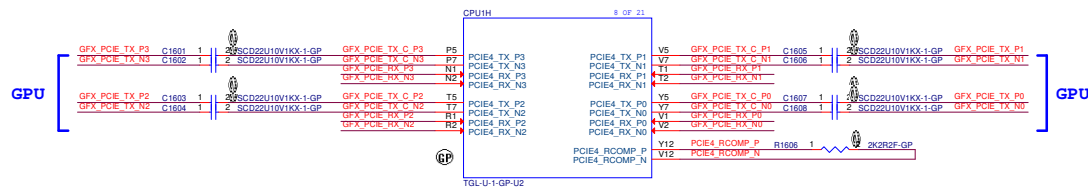
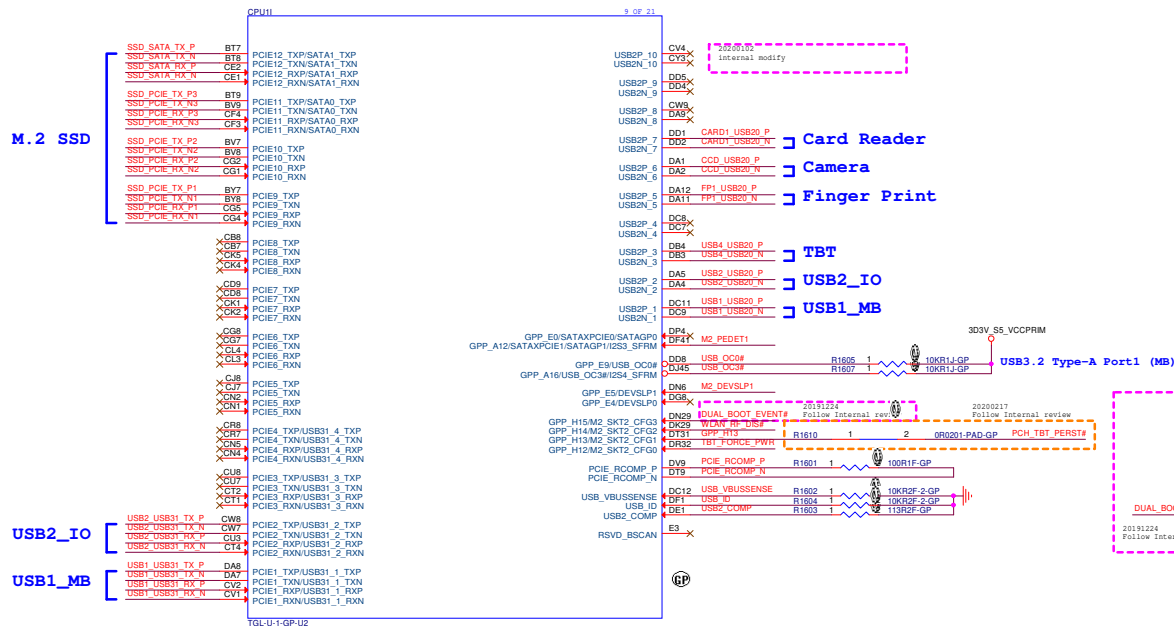
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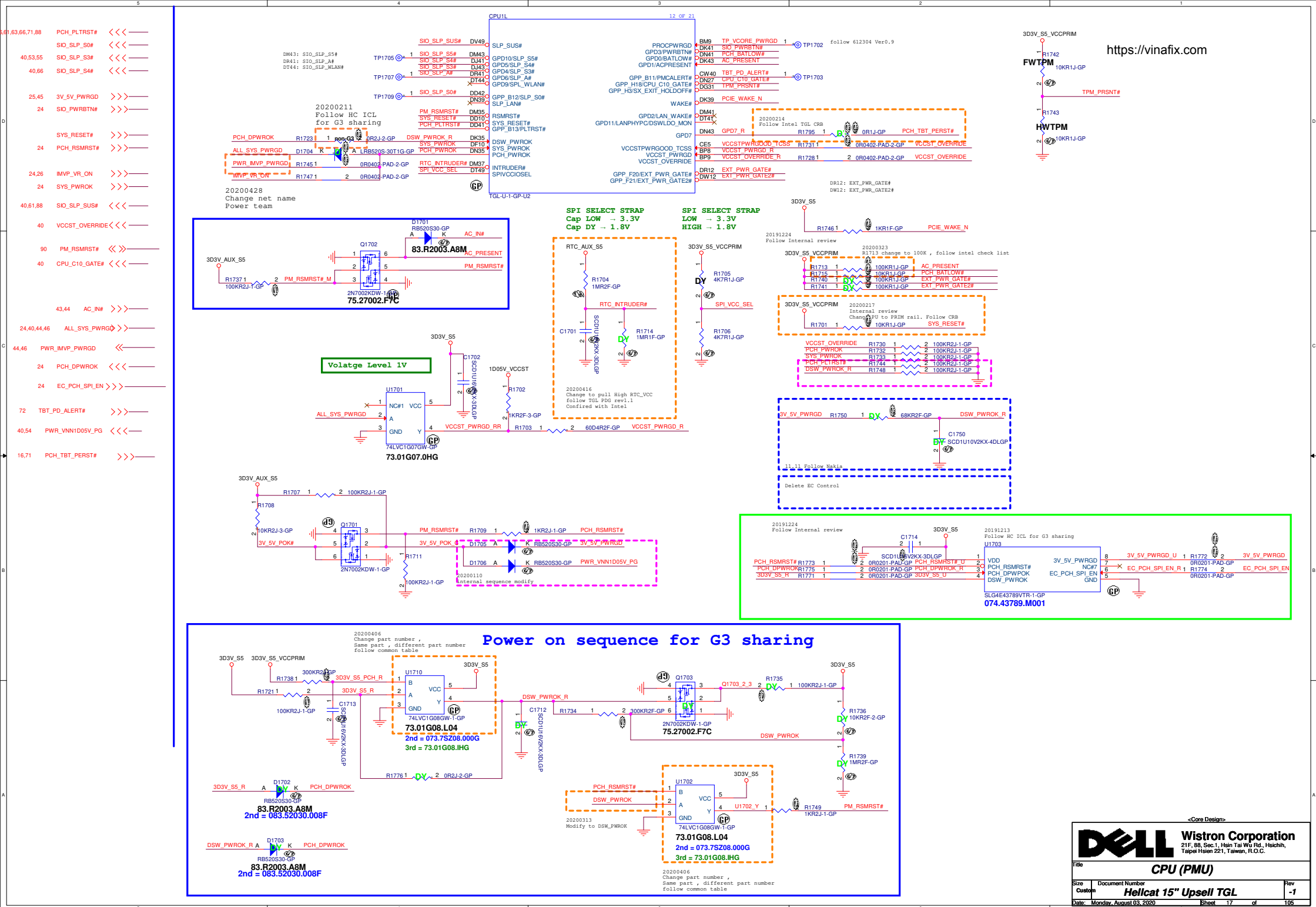
Title **DDR (RSVD) (DDR4-CHA1)**

Size A4	Document Number Hellcat 15" Upsell TGL	Rev -1
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GPIO	GPP_C5	SPI_S1	GPP_E6	GPP_B23	SPI_WP	ME_UNLOCK (GPP_R2)	CNVI debug MODES (GPP_E10)
Schematic							
High	ESPI Disable	Disable	Enable	19.2MHZ CLOCK FROM DIVIDER (DERIVED FROM 38.4MHZ CRYSTAL)	Disable	OVERRIDEN	INTEGRATED CNVI DISABLE
Low	Enable =default=	Enable	Disable	38.4MHZ CLOCK FROM DIRECT CRYSTAL (DEFAULT)	Enable	SECURITY MEASURES NOT OVERRIDEN	INTEGRATED CNVI ENABLE
GPIO	TBT LSX VCCIO conf.#0	TBT LSX VCCIO conf.#1	TBT LSX VCCIO conf.#2	TBT LSX VCCIO conf.#3	A0		GPP_E10
Schematic							
High	3.3V	3.3V	3.3V	3.3V	Disable	DFXTESTMODE DISABLED (DEFAULT)	
Low	1.8V	1.8V	1.8V	1.8V	Enable	DFXTESTMODE ENABLED	

GPP_C5	SPI_SI	GPP_E6	GPP_B23	SPI_WP	ME_UNLOCK	M.2 CNVI MODES	TBT LSX #0
ESPI OR EC LESS HIGH: ESPI IS DISABLED LOW: ESPI SELECTED WEAK INTERNAL PD 20K	BOOT HALT HIGH - DISABLED LOW - ENABLED NO INTERNAL PU/PD	JTAG ODT DISABLE LOW: JTAG ODT DISABLED HIGH: JTAG ODT ENABLED NO INTERNAL PU/PD	CPUNSSC CLOCK FREQ HIGH: 19.2MHz CLOCK FROM DIVIDER (DERIVED FROM 38.4MHz CRYSTAL) LOW: 38.4MHz CLOCK FROM DIRECT CRYSTAL (DEFAULT) WEAK INTERNAL PD 20K	CONSENT STRAP HIGH: DISABLED LOW: ENABLED NO INTERNAL PU/PD	FLASH DESCRIPTOR SECURITY OVERRIDE HIGH: OVRDEN LOW: SECURITY FEATURES NOT OVRDEN WEAK INTERNAL PD 20K	M.2 CNVI MODES LOW -> INTEGRATED CNVI ENABLE HIGH -> INTEGRATED CNVI DISABLE NO INTERNAL PU/PD	TBT LSX #PINS VCCIO CONFIGURATION HIGH: 1.5V LOW: 1.8V NO INTERNAL PU/PD
TBT LSX #1	TBT LSX #2	TBT LSX #3	A0	GPP_E10	GPP_E11		
TBT LSX #1 PINS VCCIO CONFIGURATION HIGH: 3.3V LOW: 1.8V NO INTERNAL PU/PD	TBT LSX #2 PINS VCCIO CONFIGURATION HIGH: 3.3V LOW: 1.8V NO INTERNAL PU/PD	TBT LSX #3 PINS VCCIO CONFIGURATION HIGH: 3.3V LOW: 1.8V NO INTERNAL PU/PD	A0 PERSONALITY STRAP HIGH: DISABLED LOW: ENABLED NO INTERNAL PU/PD				






```

27      HDA_SYNC_CODEC      <<<  —————
27      HDA_BITCLK_CODEC   <<<  —————
27      HDA_SDOUT_CODEC    <<<  —————
          27      HDA_SDIO   <<<  —————
          15      HDA_SDO    <<<  —————

55      DMIC_PCH_CLK_R     <<<  —————
55      DMIC_PCH_DATA_R   <<<>  —————

```

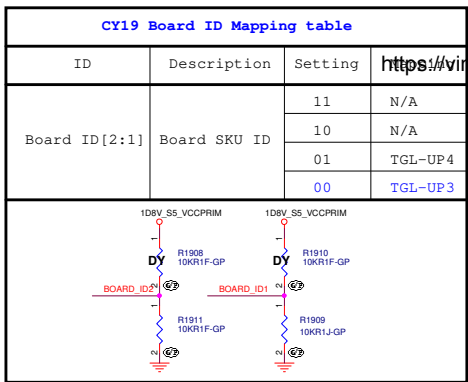
GPU

G SENSOR

RTC

BT

```
88  GPP_A11_GPU_PERST_N>>>---
```



1D8V_SS_VCCPRIM

R1906
10KR2J-3-GP
NO TBT

TBT_DET#

R1907
10KR1F-GP
Have TBT

ID	Description	Setting	Mapping
VRAM_ID[2:1]	dGPU VRAM size	11	UMA Board
		10	N/A
		01	DIS Board with 4GB VRAM
		00	DIS Board with 2GB VRAM

1D8V_SS_VCCPRIM

R2038
10KR1F-GP

UMA

VRAM_ID2

R2037
10KR1F-GP

2GB VRAM/4GB VRAM

1D8V_SS_VCCPRIM

R2035
10KR1F-GP

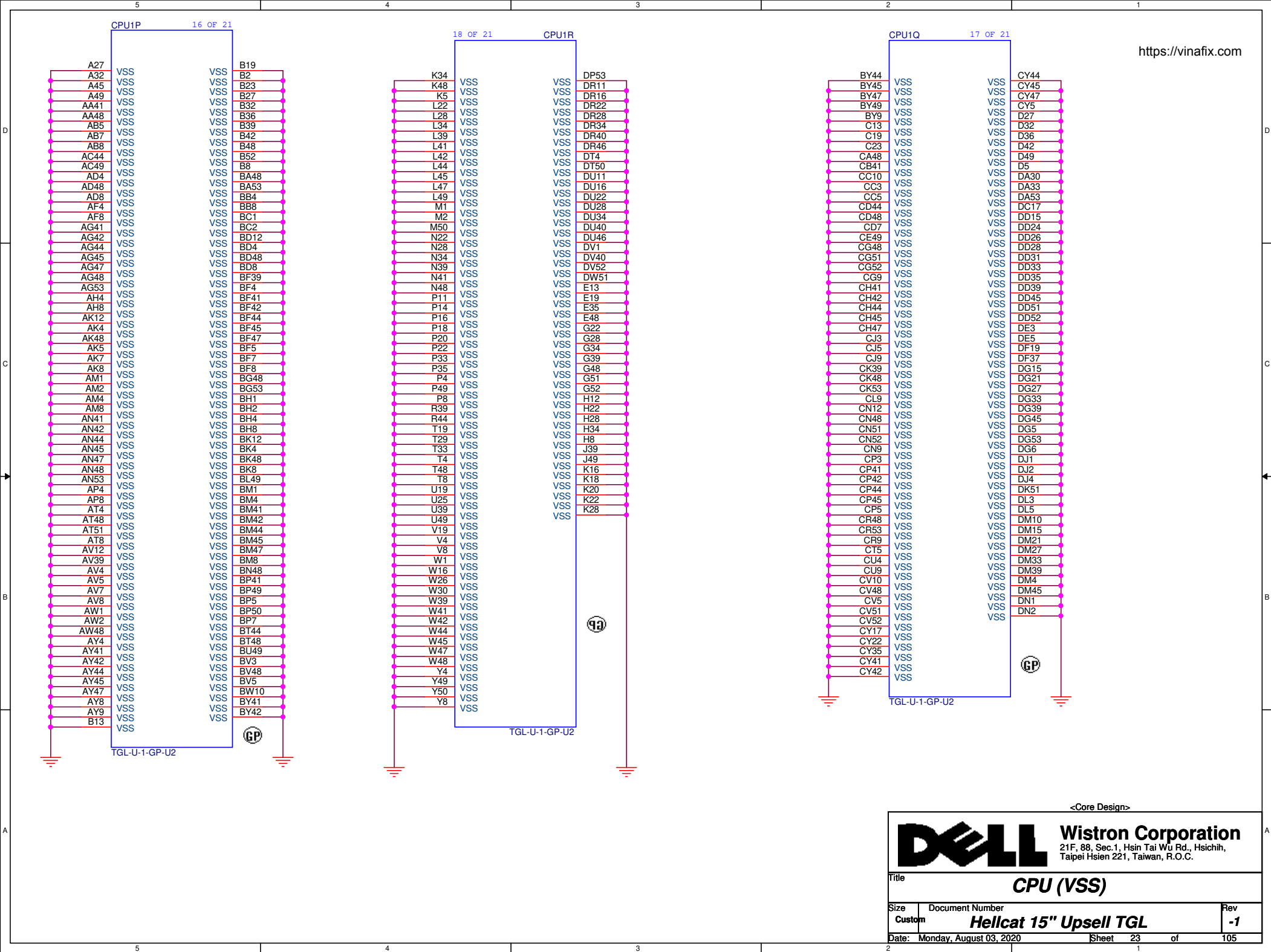
4GB VRAM/UMA

VRAM_ID1

R2034
10KR1F-GP

2GB VRAM

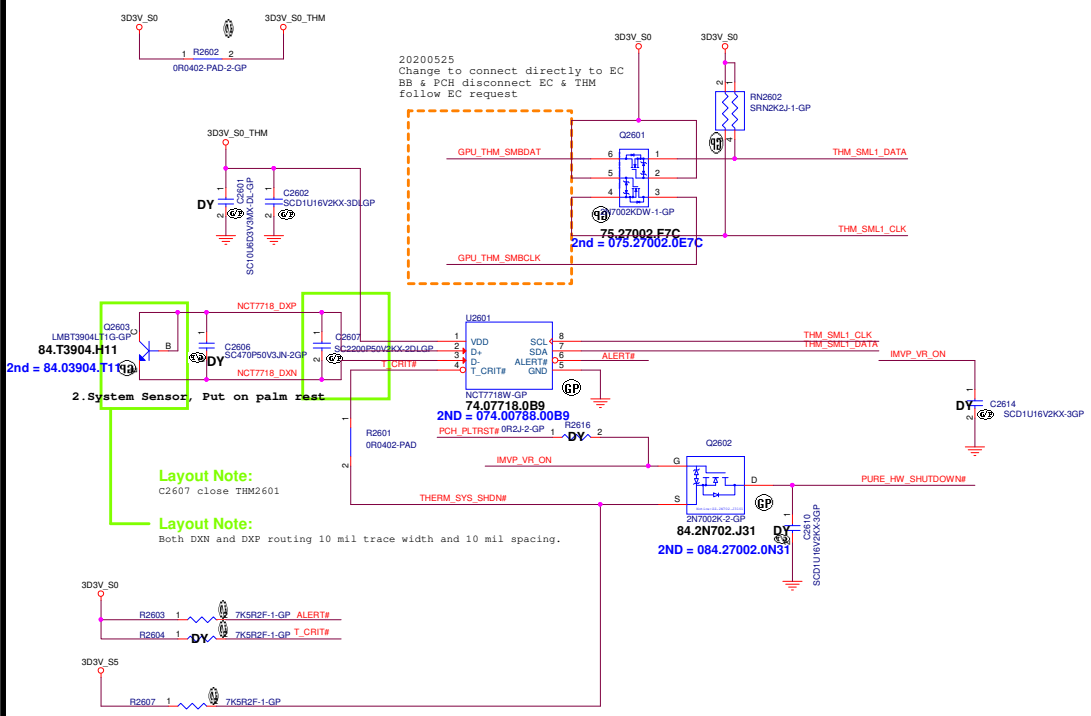




Main Func = Thermal Sensor

24 FAN_TACH1 <<< _____
24 PWM_FAN1 >>> _____
18,24 GPU_THM_SMBDAT <<< _____
18,24 GPU_THM_SMBCLK <<< _____
40 PURE_HW_SHUTDOWN# <<< _____

17,61,63,66,71,88 PCH_PLTRST# >>> _____
17,24 IMVP_VR_ON >>> _____



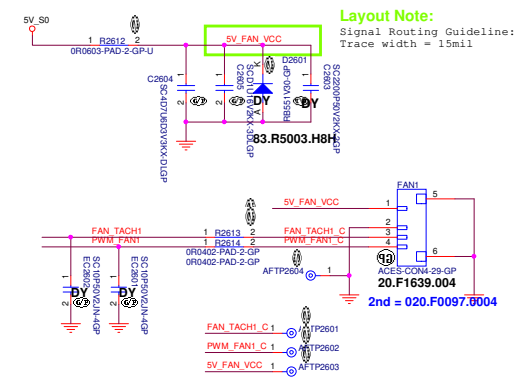
Layout Note:
C2607 close THM2601

Layout Note:
Both DXN and DXP routing 10 mil trace width and 10 mil spacing.

TEMPERATURE (°C)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

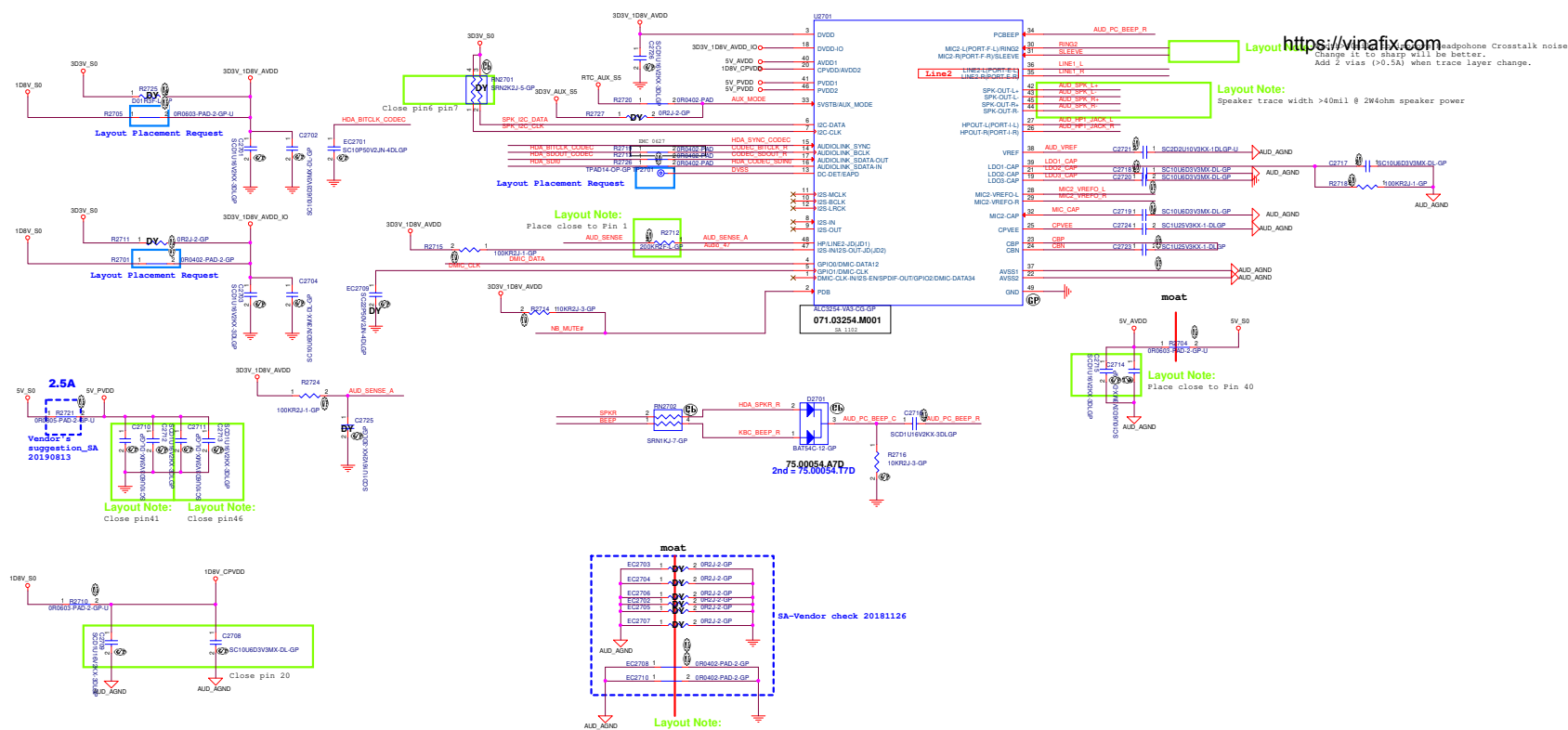
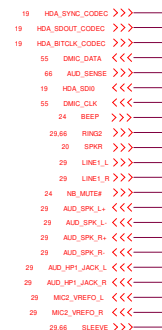
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PWM FAN1




Layout Note:
Signal Routing Guideline:
Trace width = 15mil

Main Func = Audio



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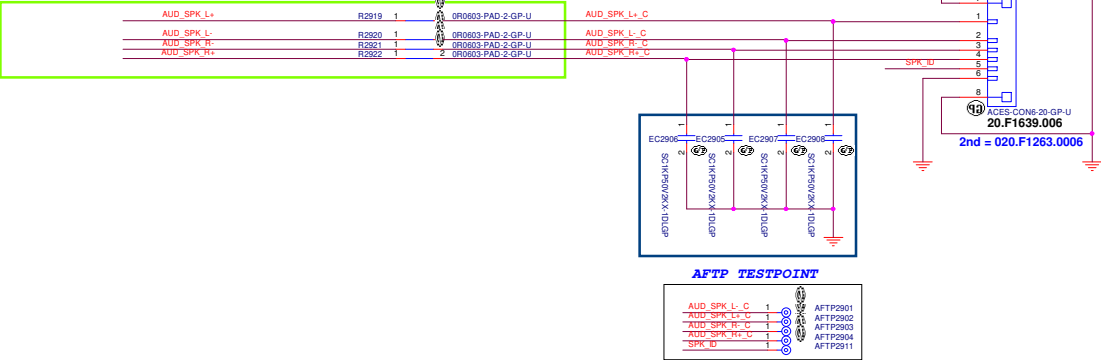
			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title					
(Reserved)					
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Main Func = Audio

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Layout Note:
Speaker trace width >40mil @ 2W4ohm speaker power



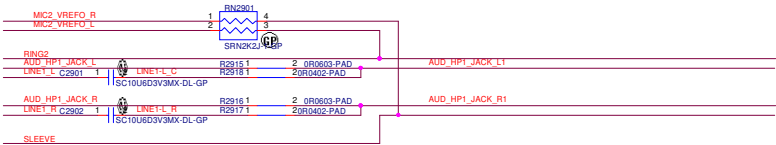
CONN Pin	Net name
Pin1	SPK_L+
Pin2	SPK_L-
Pin3	SPK_R-
Pin4	SPK_R+
Pin5	SPK_DET#
Pin6	GND

SPK_ID 1: FG
0: Veci




Line2 ->

Line2 ->



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Size

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Main Func = LAN

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Title					
LAN RTL8106					
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Main Func = LAN

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Title <i>RJ45&Transformer(RSV)</i>			
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Main Func = Card Reader

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Title

Card Reader_RTL5170(RSV)

Size
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Main Func = USB2.0

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Title

USB (RSVD) (USB 2.0 CONN)

Size

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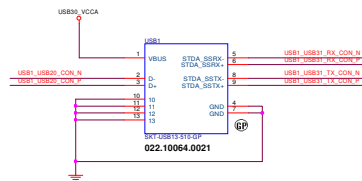
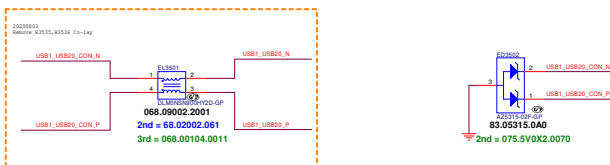
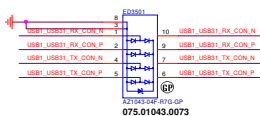
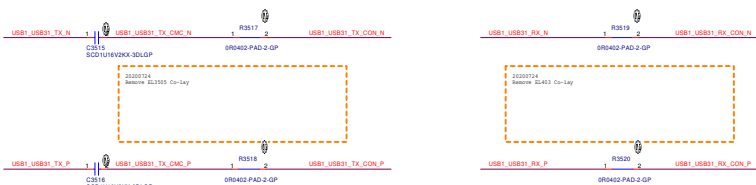
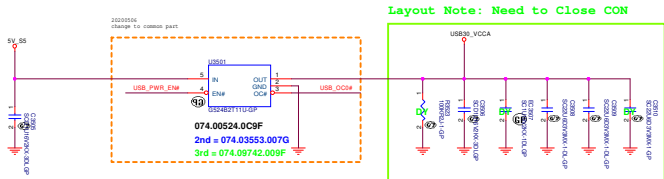
Helicat 15" Upsell TGL

-1

Main Func = USB 3.0 Port1

USB3.0 Port1

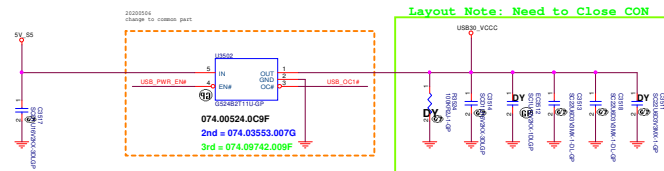
<https://vinafix.com>



Main Func = USB 3.0 Port2

USB3.0 Port2 (IO Board)


4. USB OC1# <<< _____



File		USB3.1 Gen1 Port1		
Size	Document Number	Helicat 15" Upsell TGL		Rs
Custom				
Date:	Monday, August 03, 2020	Sheet	34	of 15

(Blanking)

<Core Design>



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Title

Size
A3

Document Number
Helicat 15" Upsell TGL


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Rev
-1

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(Blanking)

<Core Design>

			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title					
USB3.0 PORT					
Size	Document Number				Rev
A4	Helicat 15" Upsell TGL				-1
Date: Monday, August 03, 2020			Sheet 37 of 105		


(Blanking)

<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size A4	Document Number Hellcat 15" Upsell TGL		Rev -1
Date: Monday, August 03, 2020		Sheet 38 of	105

(Blanking)

<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

Title

(RSVD)

Size
A3

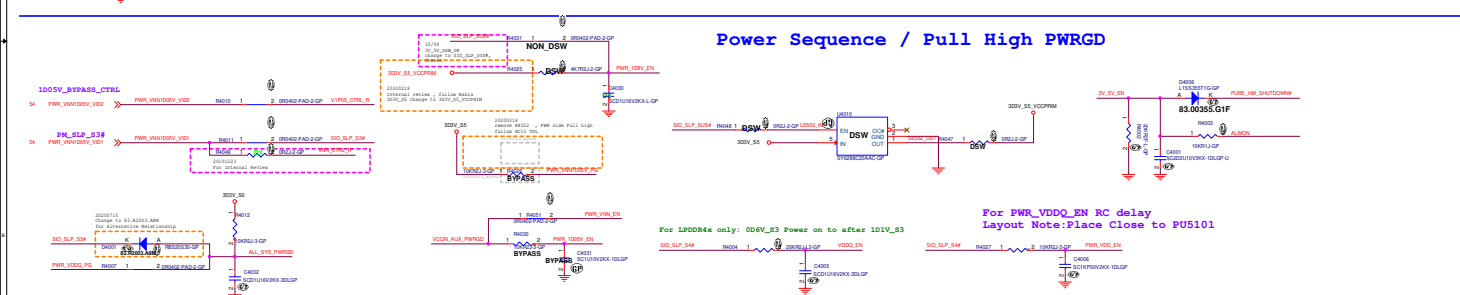
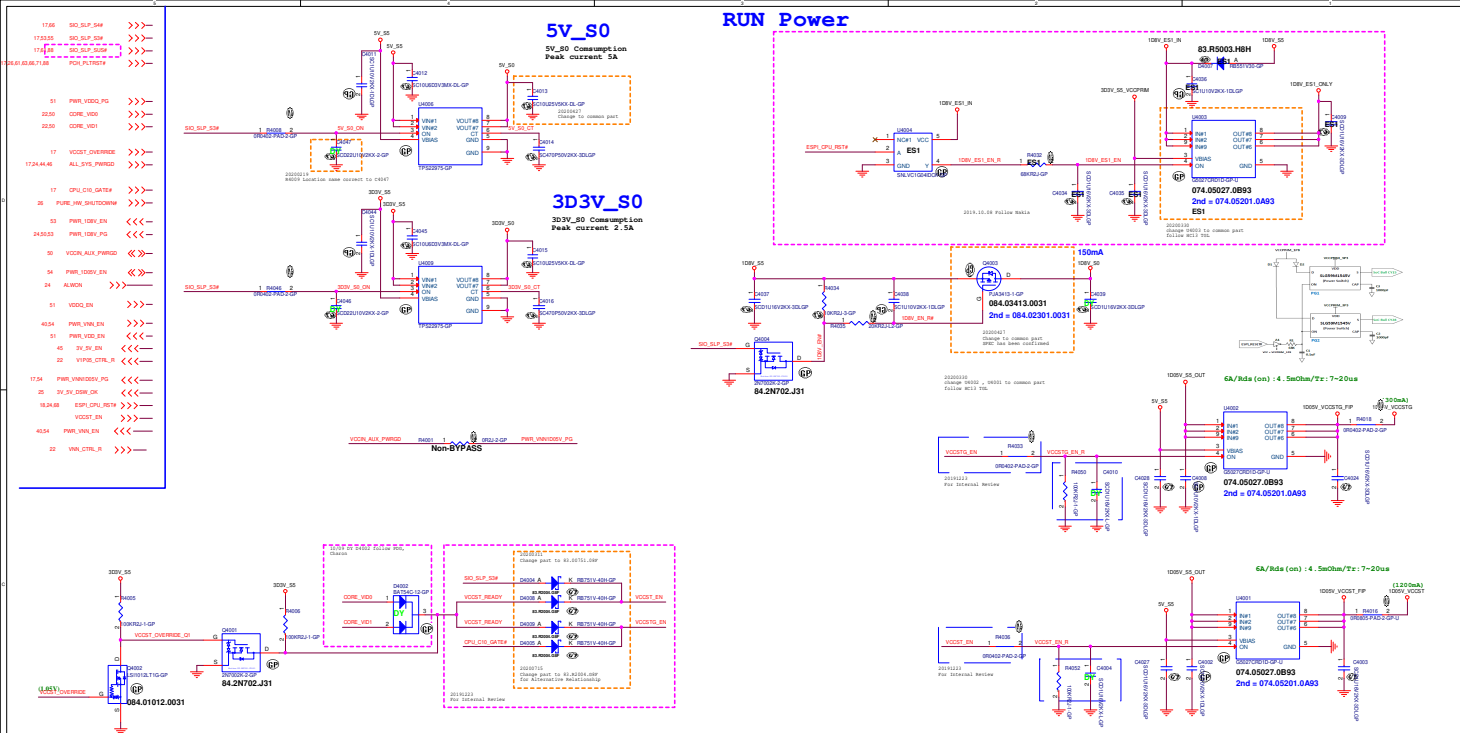
Document Number
Hellcat 15" Upsell TGL

Rev
-1

Date: Monday, August 03, 2020


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(Blanking)

<Core Design>



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Title

Sequence (RSVD)

Size
A4

Document Number

Helicat 15" Upsell TGL


Rev
-1

Date: Monday, August 03, 2020

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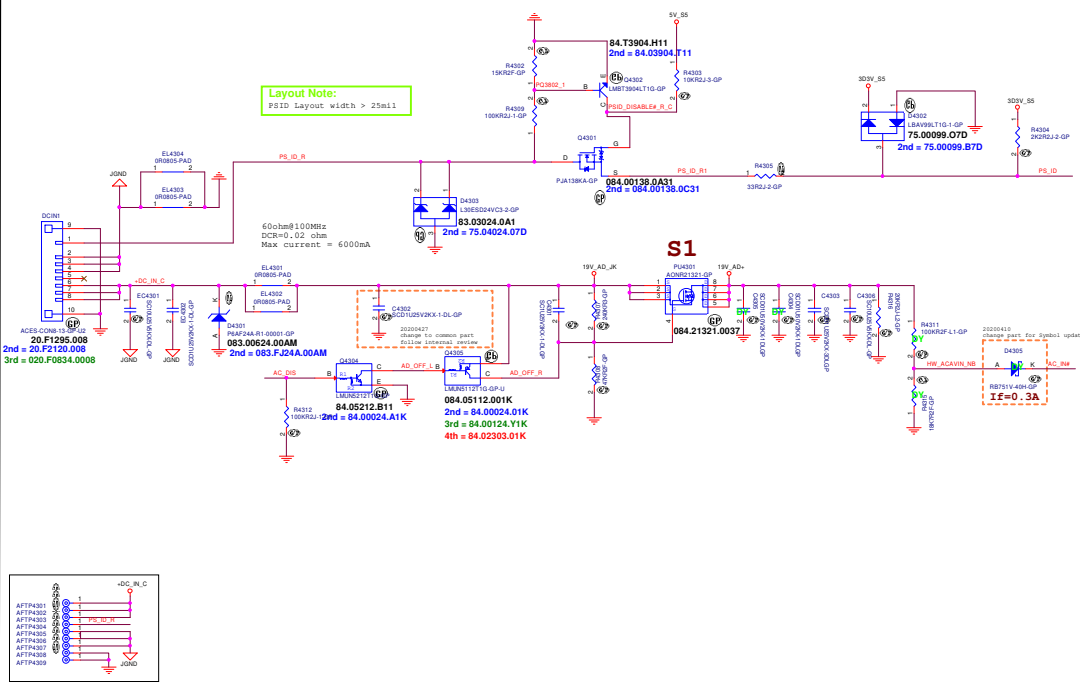
(Blanking)

<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title (RSVD)		
Size A4	Document Number Helicat 15" Upsell TGL	Rev -1
Date: Monday, August 03, 2020		Sheet 42 of 105

Main Func = ADT Input

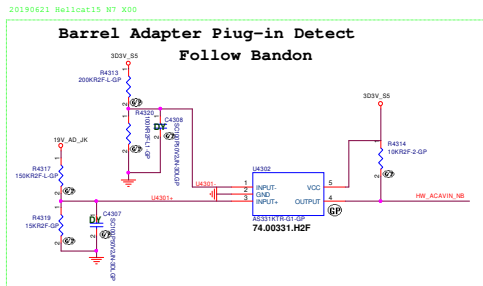
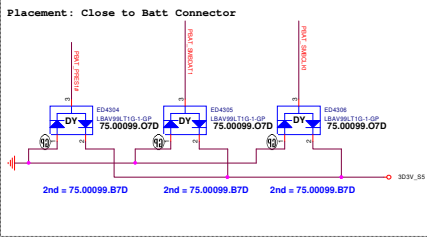
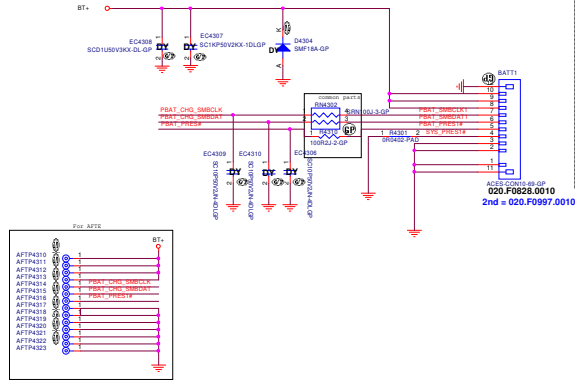
24.44 HW_ACAVIN_NB <<<—
24 PS_ID <<<—
17.44 AC_RH <<<—
24.44 AC_DS <<<—
24.44 PBAT_CHG_SMBCLK <<<—
24.44 PBAT_CHG_SMBDAT <<<—
24.44 PBAT_PRESM <<<—



Move S2 MOSFET and control logic SCH to page 44

Main Func = M-BAT Input

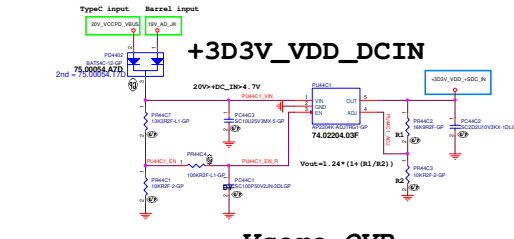
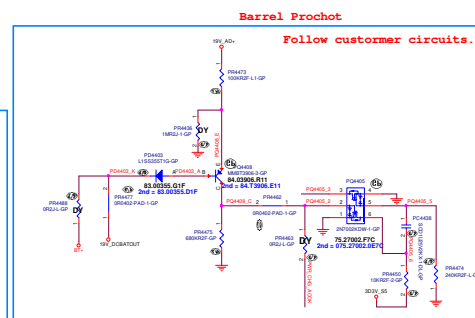
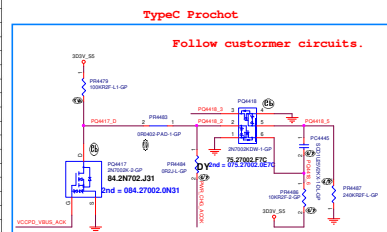
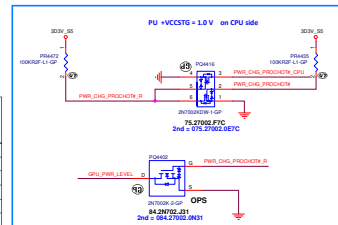
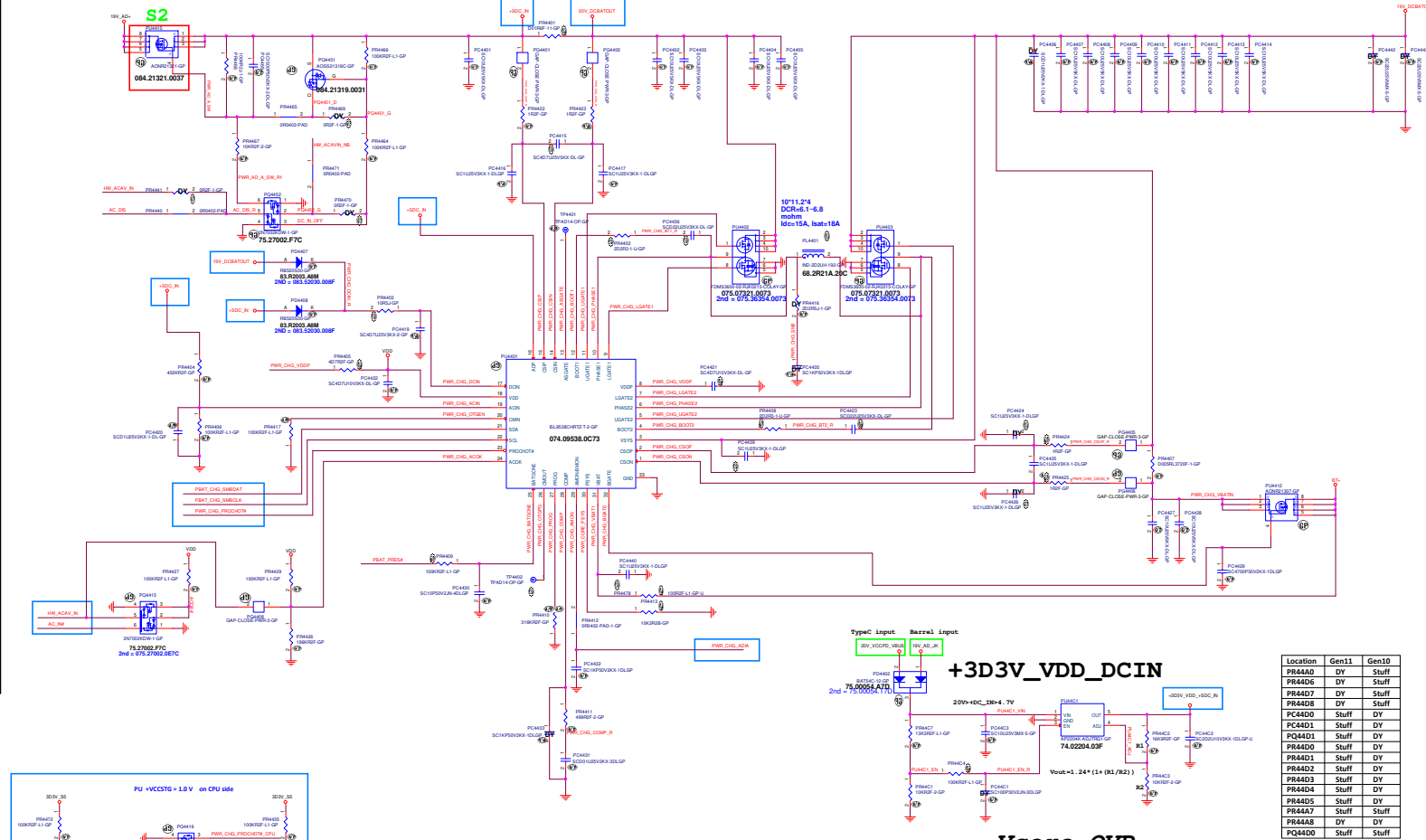
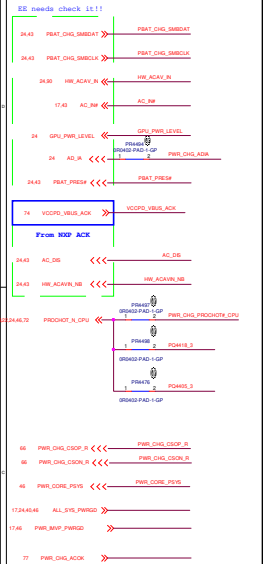
Batt Connector



ISL9538C For Charger

<https://vinafix.com>

OFFPAGE



Location	Gen11	Gen10
PR44AD	DY	Stuff
PR44DE	DY	Stuff
PR44D7	DY	Stuff
PR44D8	DY	Stuff
PC44D0	Stuff	DY
PC44D1	Stuff	DY
PR44D0	Stuff	DY
PR44D1	Stuff	DY
PR44D2	Stuff	DY
PR44D3	Stuff	DY
PR44D4	Stuff	DY
PR44D5	Stuff	DY
PR44A7	Stuff	Stuff
PR44A8	DY	DY
PC44D0	Stuff	Stuff

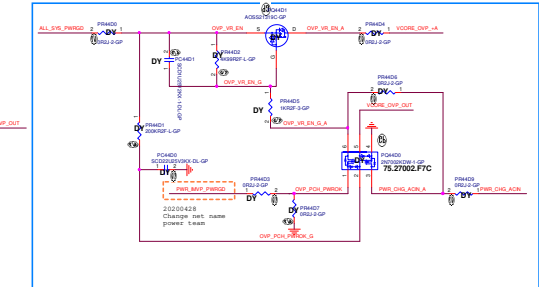
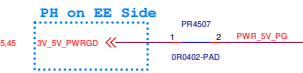


TABLE 22. PROG PIN PROGRAMMING OPTIONS							
PROG-PIN RESISTANCE (KΩ)				CELL #	DEFAULT SWITCHING FREQUENCY	Autonomous charging	DEFAULT ACINRES1 Reg(A)
MIN	TYP	MAX					
0	0	0	0	1	733kHz	No	0.476
8.45	0	0	0	1	733kHz	No	1.5
14.7	0	0	0	1	1MHz	No	0.476
22.0	0	0	0	1	1MHz	No	0.476
28.0	0	0	0	1	733kHz	Yes	0.476
35.7	0	0	0	1	733kHz	Yes	1.5
43.2	0	0	0	2	733kHz	Yes	1.5
52.3	0	0	0	2	733kHz	Yes	0.476
61.9	0	0	0	2	1MHz	No	0.476
71.5	0	0	0	2	1MHz	No	1.5
82.5	0	0	0	2	733kHz	No	1.5
93.5	0	0	0	2	733kHz	No	0.476
105	0	0	0	3	733kHz	No	0.476
118	0	0	0	3	733kHz	No	1.5
133	0	0	0	3	1MHz	No	1.5
147	0	0	0	3	1MHz	No	0.476
162	0	0	0	3	733kHz	Yes	0.476
178	0	0	0	3	733kHz	Yes	1.5
196	0	0	0	4	733kHz	Yes	1.5
215	0	0	0	4	733kHz	Yes	0.476
237	0	0	0	4	1MHz	No	0.476
261	0	0	0	4	1MHz	No	1.5
287	0	0	0	4	733kHz	No	1.5
316	0	0	0	4	733kHz	No	0.476
348	0	0	0	1	733kHz	No	0.476

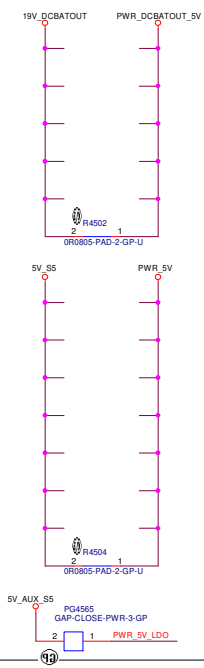
SSID = PWR.Plane.Regulator_5V

OFFPAGE-Signal

PH on EE Side

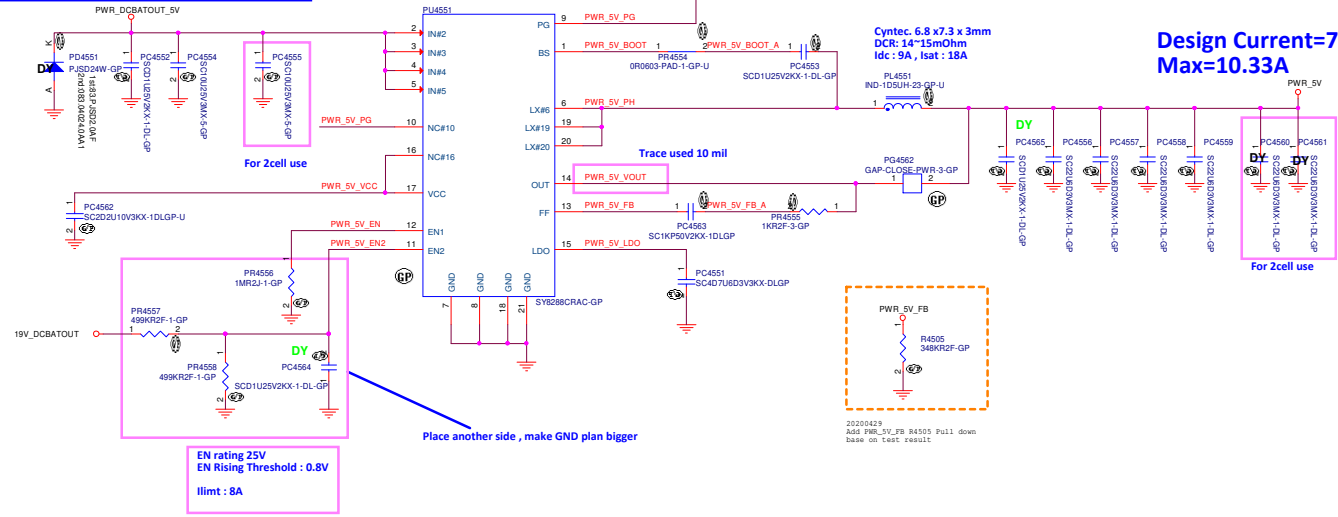
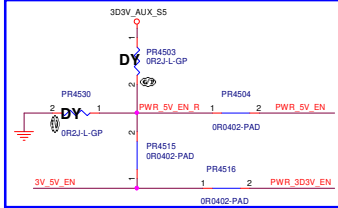


OFFPAGE-GAP



SY8288C For 5V

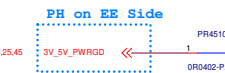
https://vinafix.com



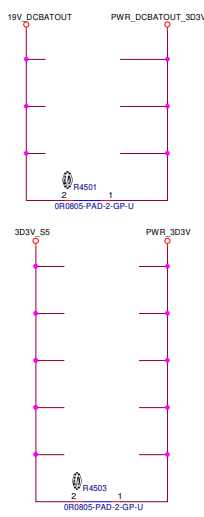
Design Current=7.231A
Max=10.33A

SSID = PWR.Plane.Regulator_3D3V

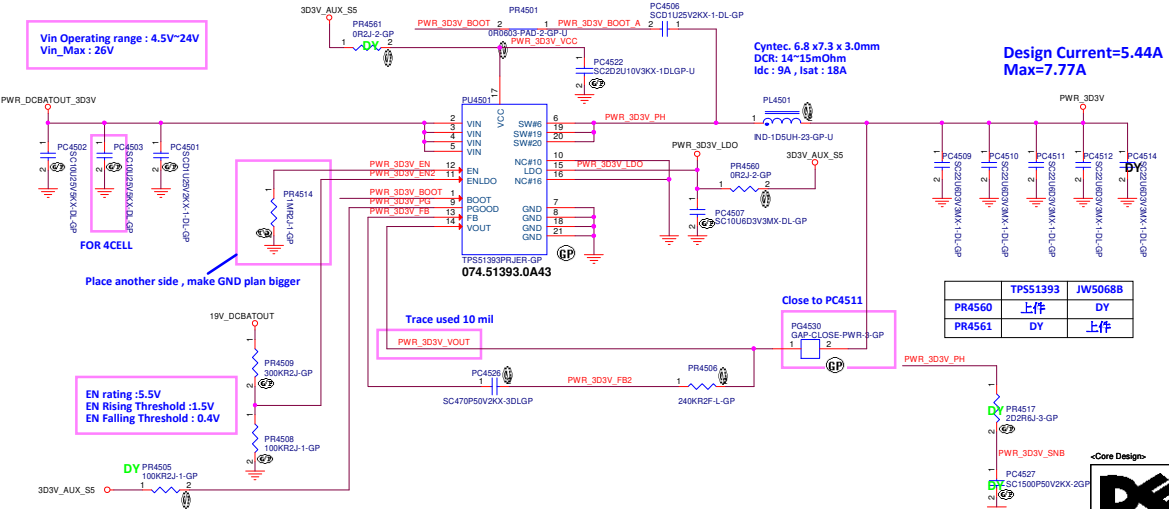
OFFPAGE-Signal



OFFPAGE-GAP



TPS51393 For 3D3V



Design Current=5.44A
Max=7.77A

	TPS51393	JW5068B
PR4560	上作	DY
PR4561	DY	上作

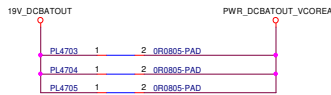
Main Func = VCCIN

OFFPAGE

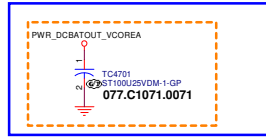
PWR_VCORE_UGATE1>> PWR_VCORE_UGATE1
PWR_VCORE_PHASE1>> PWR_VCORE_PHASE1
PWR_VCORE_LGATE1>> PWR_VCORE_LGATE1

PWR_VCORE_UGATE2>> PWR_VCORE_UGATE2
PWR_VCORE_PHASE2>> PWR_VCORE_PHASE2
PWR_VCORE_LGATE2>> PWR_VCORE_LGATE2

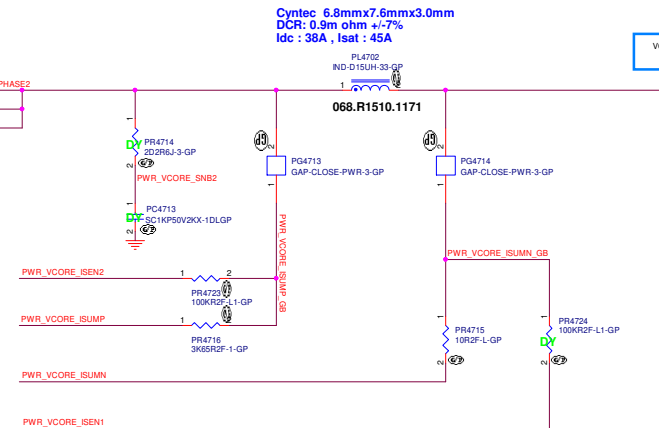
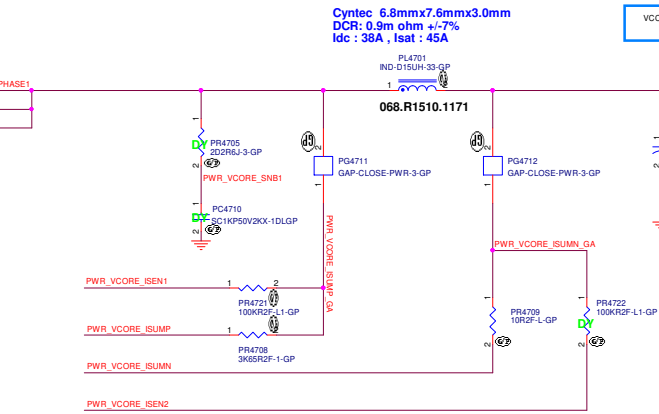
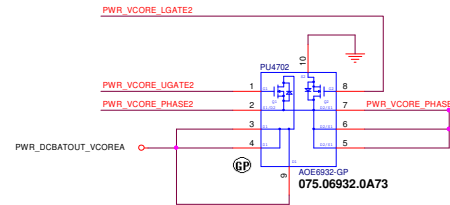
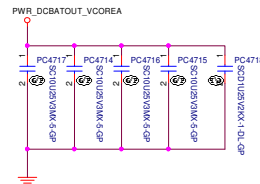
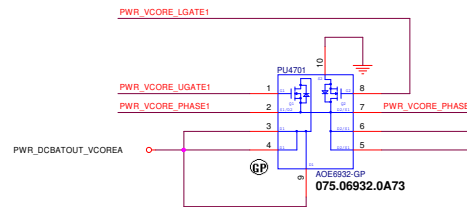
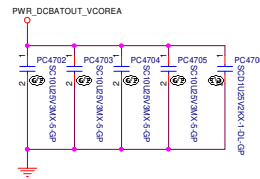
PWR_VCORE_ISEN2 << PWR_VCORE_ISEN2
PWR_VCORE_ISEN1 << PWR_VCORE_ISEN1
PWR_VCORE_ISUMP << PWR_VCORE_ISUMP
PWR_VCORE_ISUMN << PWR_VCORE_ISUMN



FOR acoustic noise



20200514
330 25V Change to 1000 25V
Follow internal review




<https://vinafix.com>

TGL_U42 28W
Performance
TDC=38A
ICCMAX=62A

Main Func = CPU_CORE

<https://vinafix.com>

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Title

POWER (IMVP9_RESERVE)

Size

A3

Document Number

Helicat 15" Upsell TGL

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-1

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<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

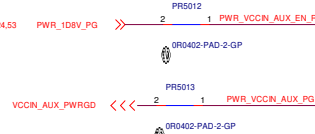
Title **POWER (RSVD)**

Size A	Document Number <i>Hellcat 15" Upsell TGL</i>	Rev -1
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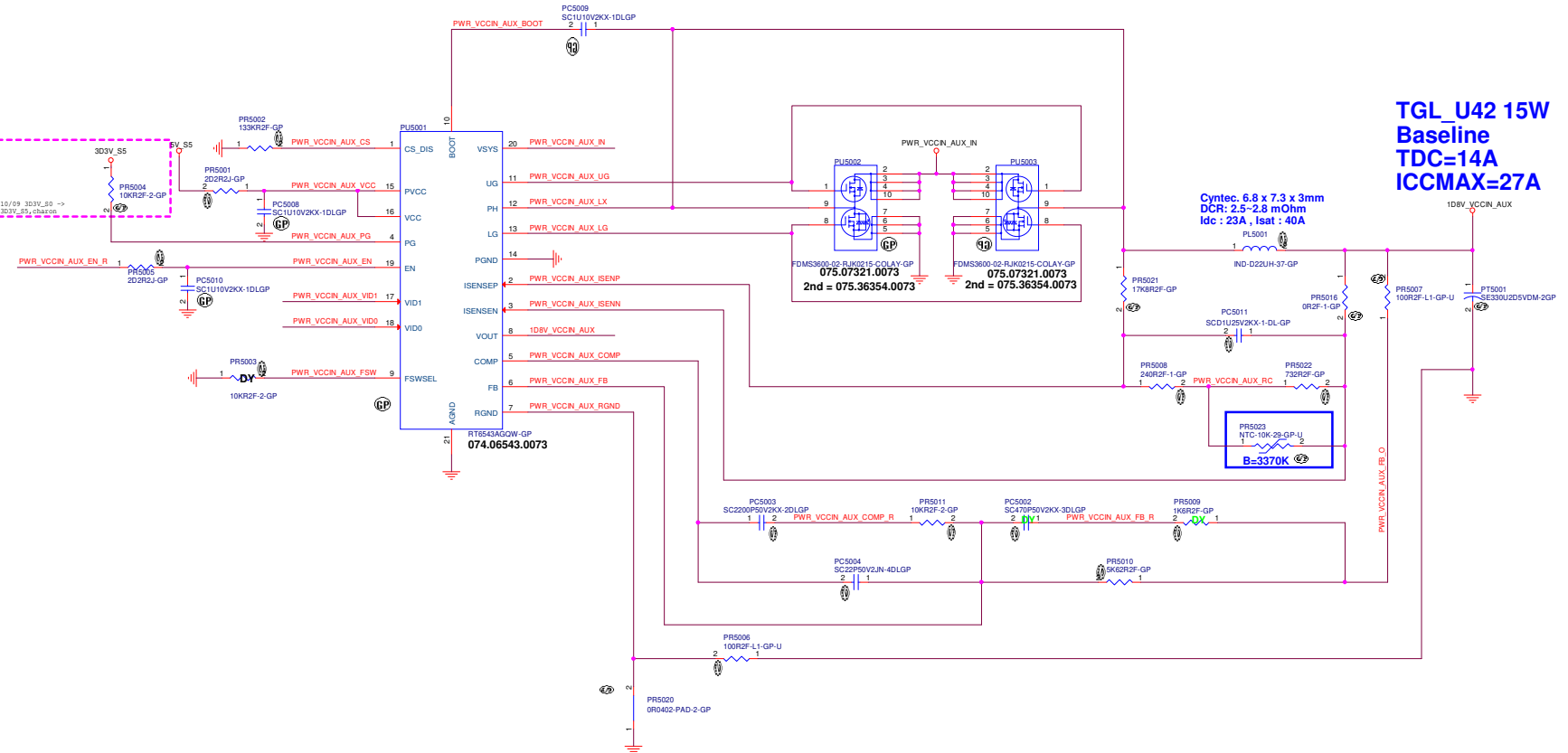
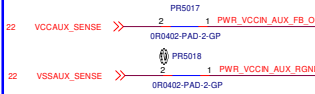
Main Func = VCCIN_AUX

OFFPAGE

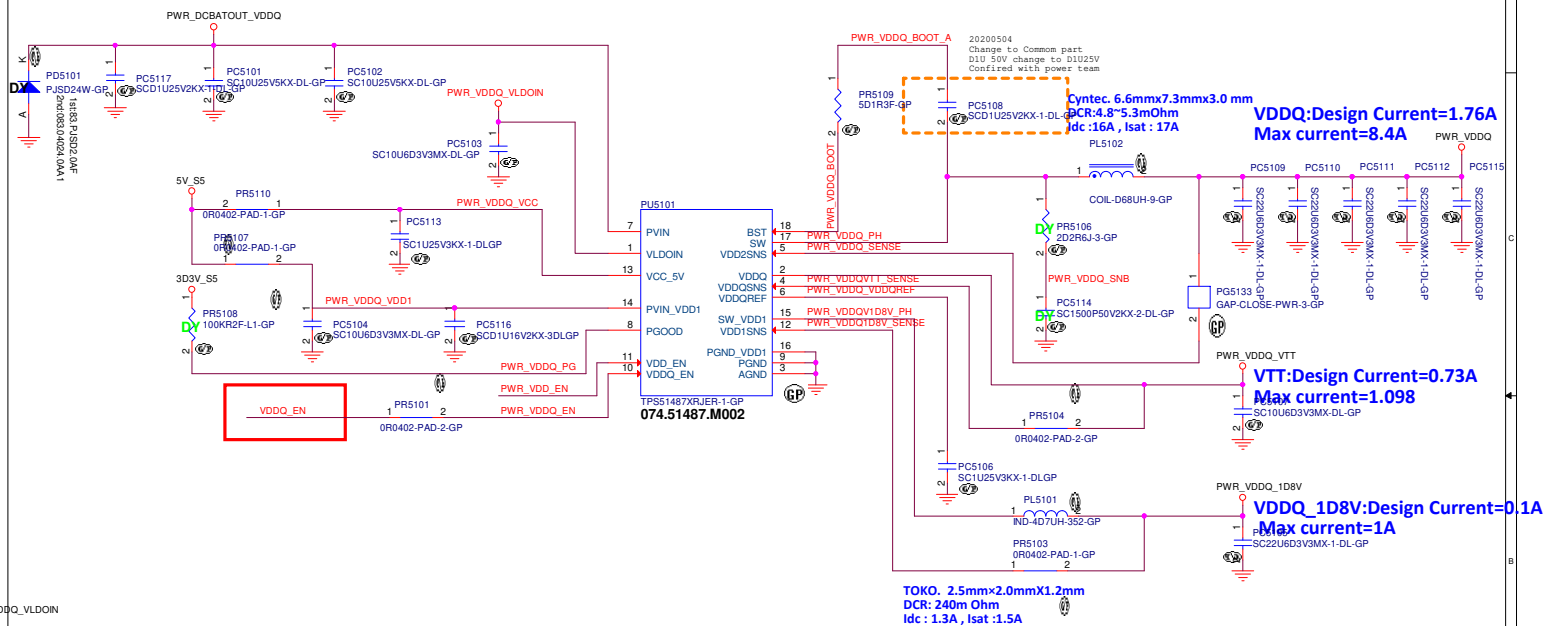
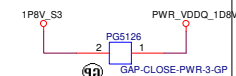
VID



VCCIN_AUX_SENSE



PWR_VDDQ_PG



<Core Design>



Title POWER (TPS51487X_VDDQVTT)			
Size Custom	Document Number Hellicat 15" Upsell TGL		Rev -1
Date: Monday, August 03, 2020	Sheet	51 of	105

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<Core Design>



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Title

Power (RSVD)

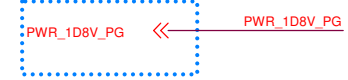
Size B	Document Number Helicat 15" Upsell TGL	Rev -1
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Date: Monday, August 03, 2020	Sheet 1	52 of 105
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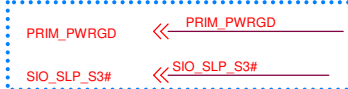
Main Func = 1D8V/1D2V

OFFPAGE

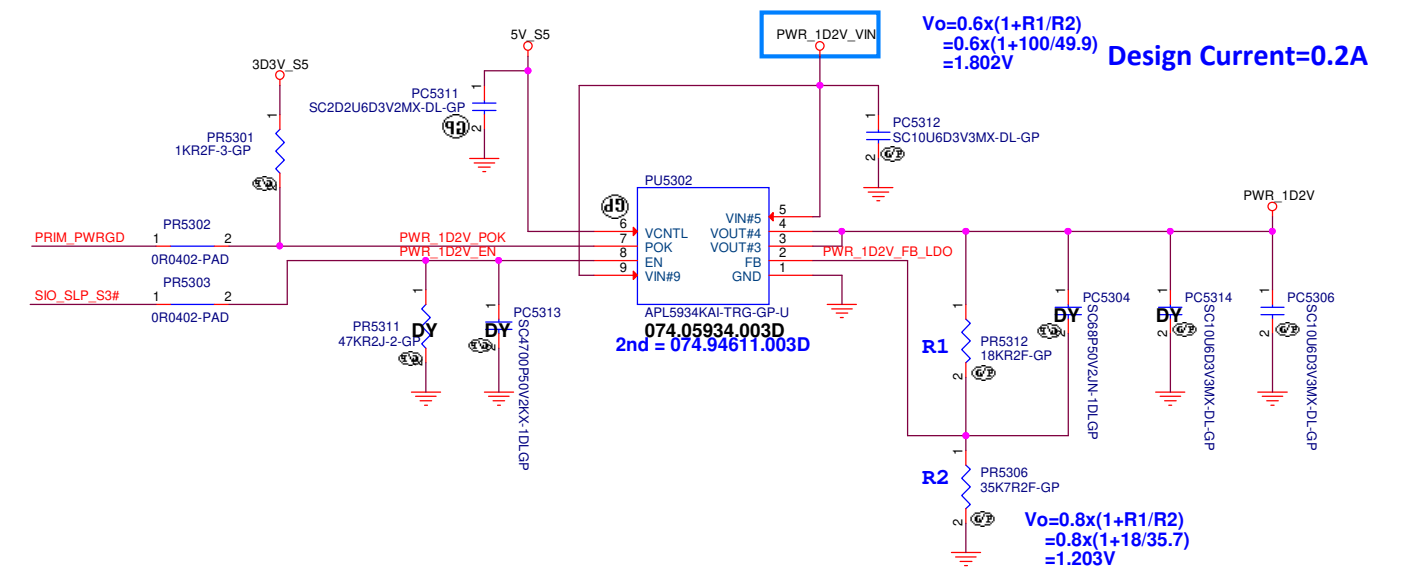
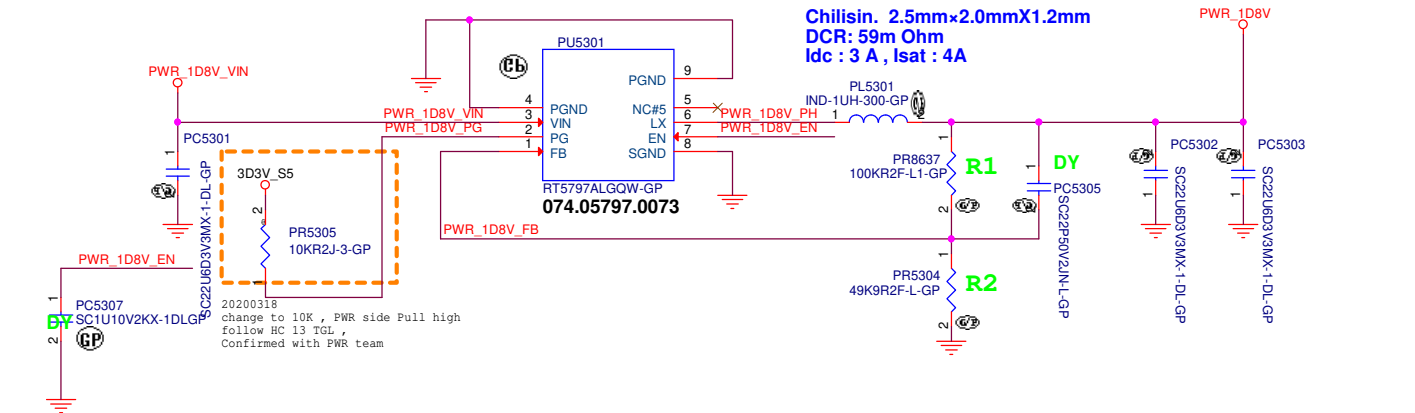
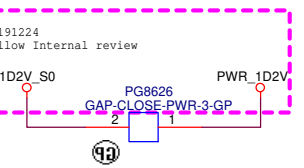
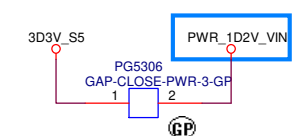
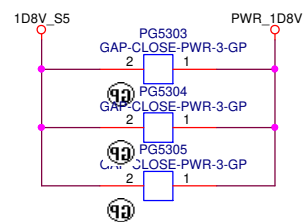
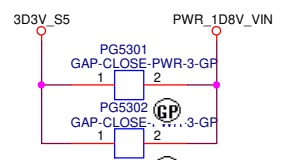
PH on EE Side



EE confirm



OFFPAGE_GAP



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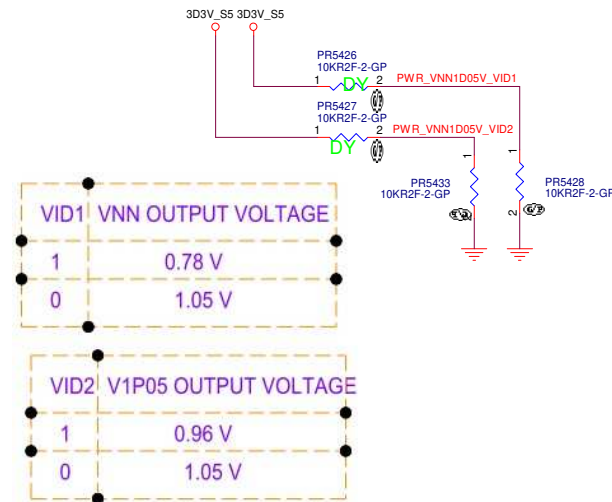
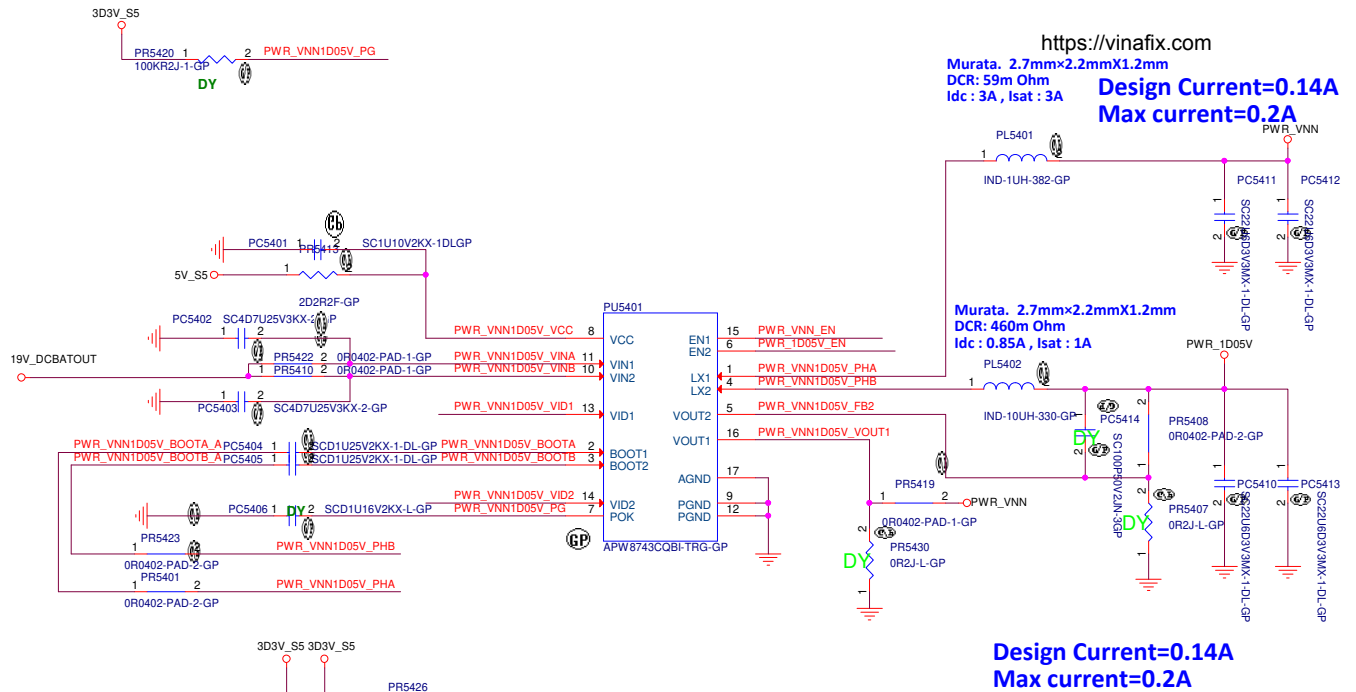
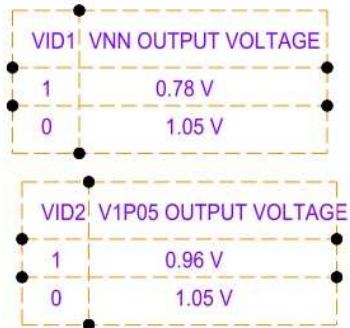
POWER (RT5797_1D8V_S5)

Document Number
Hellcat 15" Upsell TGL

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PH on EE Side



Design Current=0.14A
Max current=0.2A

<https://vinafix.com>

Murata. 2.7mm×2.2mmX1.2mm

DCR: 59m Ohm
Idc : 3A , Isat : 3A

Design Current=0.14A
Max current=0.2A

Murata. 2.7mmx2.2mmX1.2mm

DCR: 460m Ohm
Idc : 0.85A , Isat :

PL5402

<Core Design>

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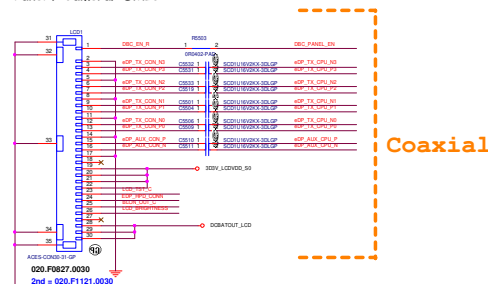
Title	POWER (RT5797_1D8V_S5)
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Size	Document Number	Rev
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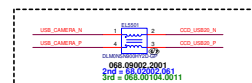
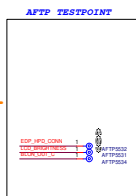
Custom **Hellcat 15" Upsell TGL** -1

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Panel / Camera/ DMIC



Coaxial



Sensor

Touch Panel

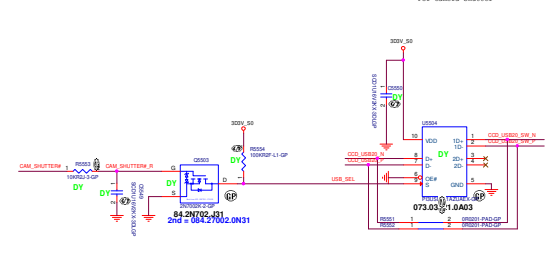
Camera

TP PIN DEFINE

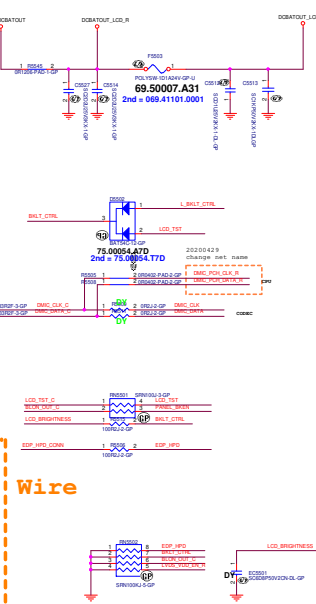
1	VUSB_3.3V
2	NC
3	SCL
4	SDA
5	UA_INT
6	RESET
7	Report Switch
8	NC
9	GND
10	GND



CAMERA USB2.0 SWITCH

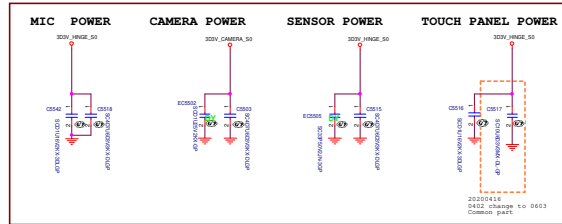
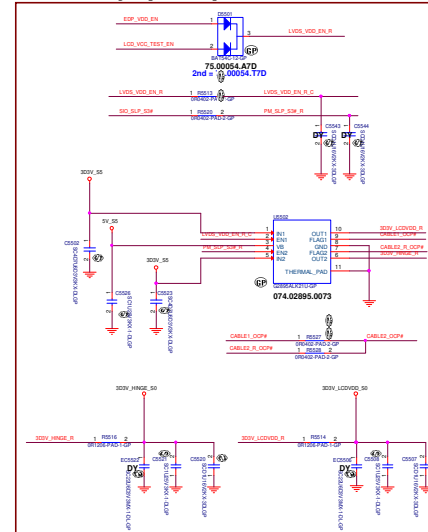


INVERTER POWER

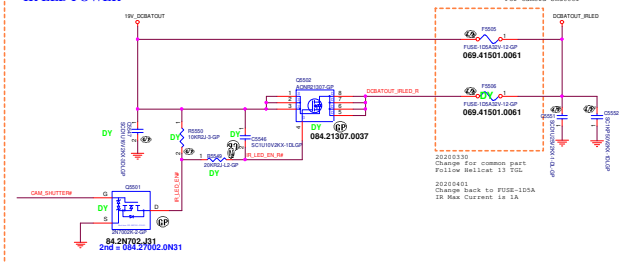


Wire

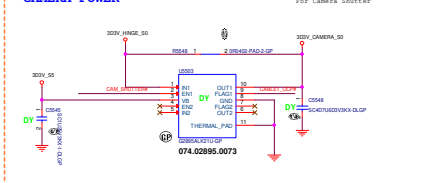
Hinge up cable protection




IR LED POWER



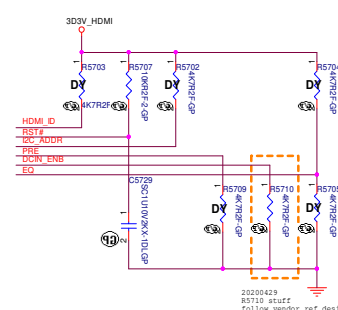
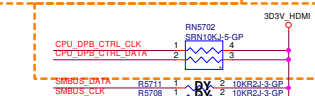
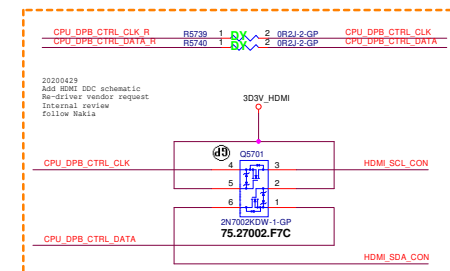
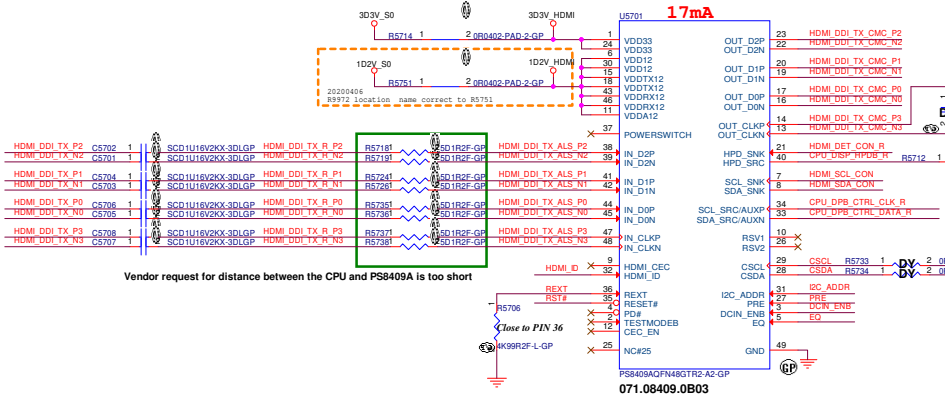
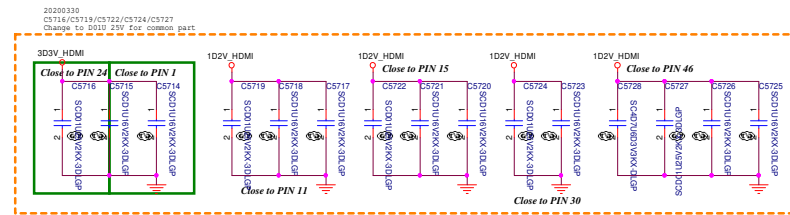
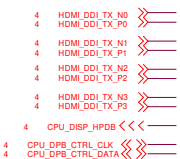
CAMERA POWER



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Title			
Display (CRT/IRP Camera)			
Size A2	Document Number	Helicat 15" Upstream TGL	Rev -1
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5
Main Func = HDMI



<https://vinafix.com>

```

IS coupling enable: Internal pull up, 3.3V I/O.
  IS coupling input
  H Default, no coupling input

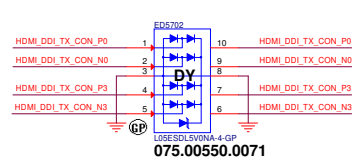
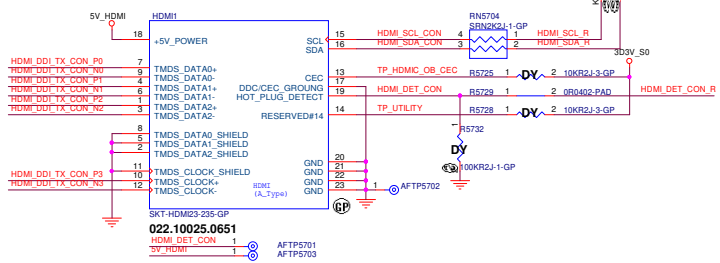
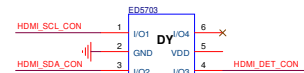
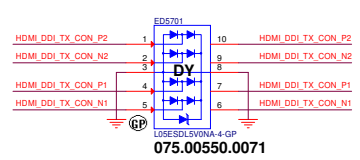
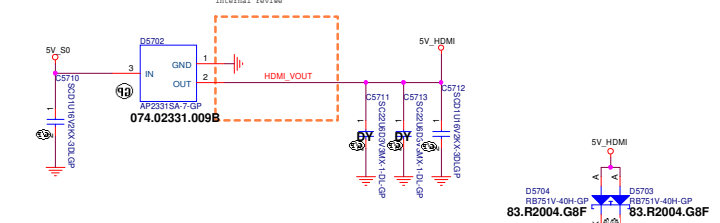
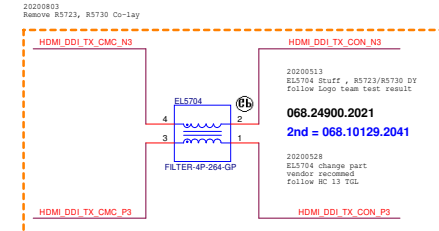
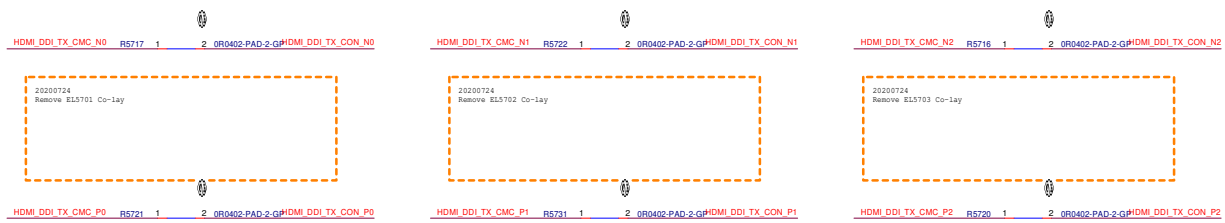
Answer evaluation settings: Internal pull up, 3.3V I/O.
  H Compensation for channel loss up to 1248
  H Default, Compensation for channel loss 0.000 170
  M Compensation for channel loss up to 1248

Output preemphasis settings: Internal pull up, 3.3V I/O.
  L Pre-emphasis <2.500
  H Default, no Pre-emphasis


120 Slave Address settings: Internal pull down, 3.3V I/O.
  L Default, slave address 0x00-0x0F
  H Alternative slave bus 0x00-0x0F, 0x00-0x0F.

HDMI ID enable : Internal pull down, 3.3V I/O.
  L Default, HDMI ID enable
  H HDMI ID disable

```



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Custom

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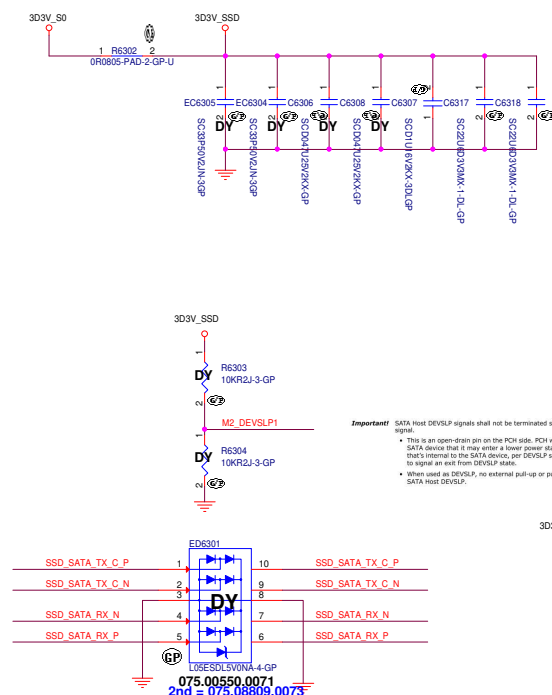
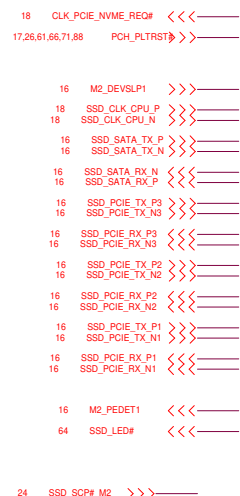


Table 13-12. SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express® Gen 2 Only	PCI Express® Gen 3 Only	SATA Only	PCI Express® Gen 2/ SATA	PCI Express® Gen 3/ SATA
Processor Tx	None	220 nF	10 nF	None	220 nF
Processor Rx	None	None	10 nF ²	None	None ³

Notes:

- Design Constraint: For PCIe only application, both Tx and Rx channels need to have 10 nF capacitors on the motherboard. This option supports all SATA devices. However, the 1x10 nF capacitor can be removed if the DC coupled ODDs / Devices are NOT used.
- Design Constraint: For PCIe® Gen 2/ SATA configuration, motherboard Tx requires a 100 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
- Design Constraint: For PCIe® Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**

¹For SATA applications, refer to the Chapter 3, "General Differential Signals Design Guidelines" along with the additional guidelines in this section for all design optimization guidelines.

²Design Constraint: For PCIe® lane that needs to support either PCIe® Gen2 devices or PCIe® Gen3 devices, follow the design constraint, remove capacitor, motherboard Tx requires a 100 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**

³Design Constraint: For SATA applications, refer to the Chapter 3, "General Differential Signals Design Guidelines" along with the additional guidelines in this section for all design optimization guidelines.

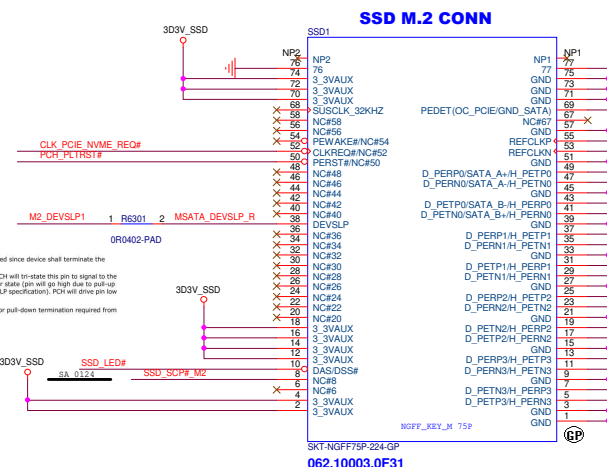
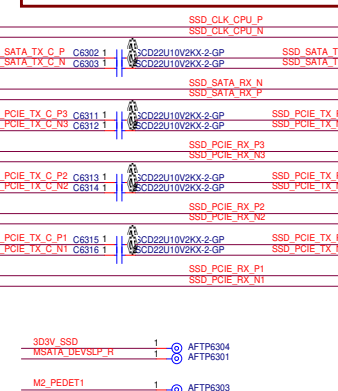
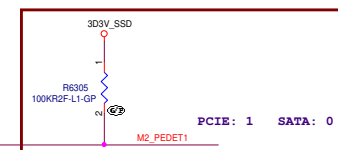


Table 48. Socket 3 SSD Pin-Out (Mechanical Key M) On Platform

Index	Key	Value
1	1	1
2	2	2
3	3	3
4	4	4
5	5	5
6	6	6
7	7	7
8	8	8
9	9	9
10	10	10
11	11	11
12	12	12
13	13	13
14	14	14
15	15	15
16	16	16
17	17	17
18	18	18
19	19	19
20	20	20
21	21	21
22	22	22
23	23	23
24	24	24
25	25	25
26	26	26
27	27	27
28	28	28
29	29	29
30	30	30
31	31	31
32	32	32
33	33	33
34	34	34
35	35	35
36	36	36
37	37	37
38	38	38
39	39	39
40	40	40
41	41	41
42	42	42
43	43	43
44	44	44
45	45	45
46	46	46
47	47	47
48	48	48
49	49	49
50	50	50
51	51	51
52	52	52
53	53	53
54	54	54
55	55	55
56	56	56
57	57	57
58	58	58
59	59	59
60	60	60
61	61	61
62	62	62
63	63	63
64	64	64
65	65	65
66	66	66
67	67	67
68	68	68
69	69	69
70	70	70
71	71	71
72	72	72
73	73	73
74	74	74
75	75	75
76	76	76
77	77	77
78	78	78
79	79	79
80	80	80
81	81	81
82	82	82
83	83	83
84	84	84
85	85	85
86	86	86
87	87	87
88	88	88
89	89	89
90	90	90
91	91	91
92	92	92
93	93	93
94	94	94
95	95	95
96	96	96
97	97	97
98	98	98
99	99	99
100	100	100

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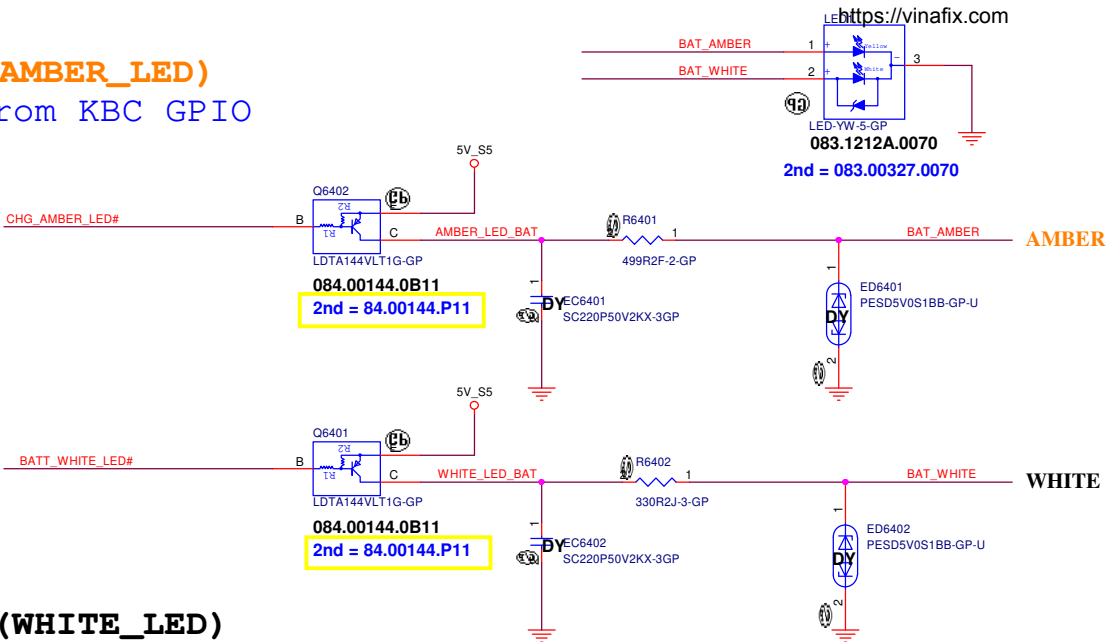
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Main Func = Power BTN

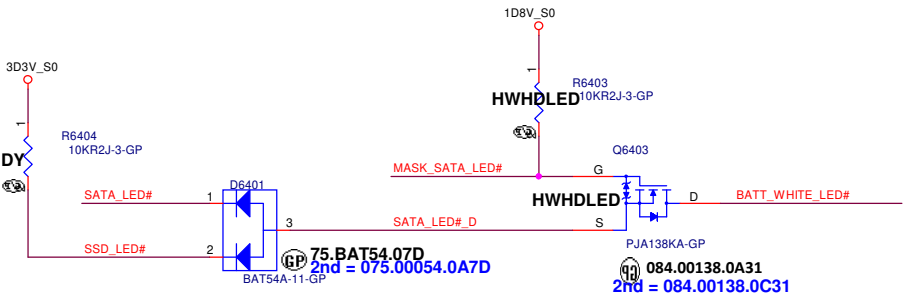
24,90 CHG_AMBER_LED# >>>—
24 BATT_WHITE_LED# >>>—

Battery LED1 (AMBER_LED)
Low activated from KBC GPIO



Battery LED2 (WHITE_LED)
Low activated from KBC GPIO

18 SATA_LED# >>>—
63 SSD_LED# >>>—
24 MASK_SATA_LED# >>>—



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Title: **LED Board&Power Button**

Size: A3 Document Number: **Helicat 15" Upsell TGL** Rev: **-1**

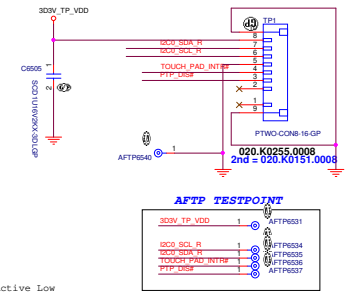
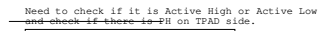
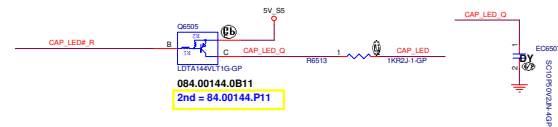
Date: Monday, August 03, 2020 Sheet: 64 of 105

Main Func = TPAD

«Core Design»



File			
Key Board&Touch Pad			
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Pin number	Pin name
1	VDD
2	DAT (I2C)
3	CLK (I2C)
4	GND
5	ATTN
6	GPIO
7	DAT (PS2)
8	CLK (PS2)

Main Func = IO Connector

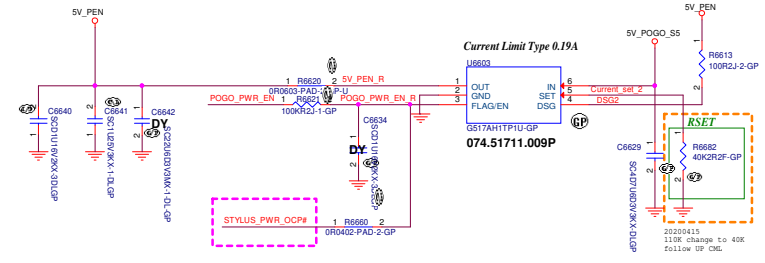
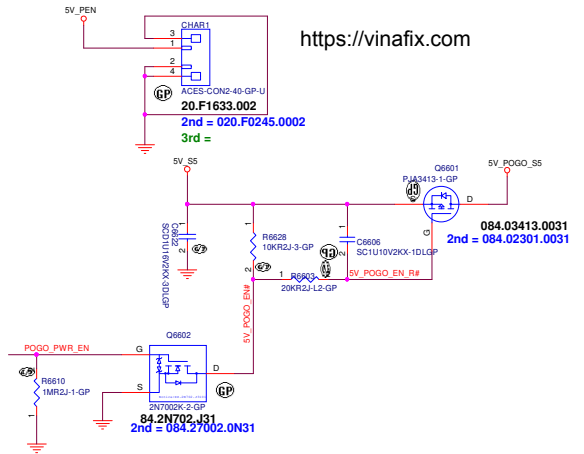
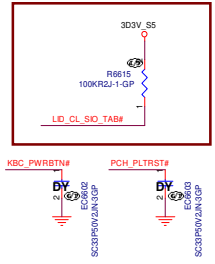
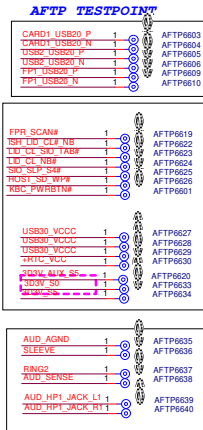
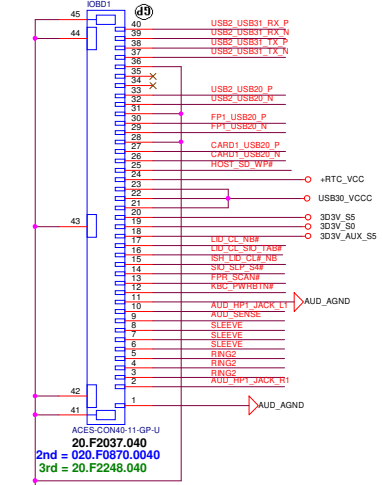
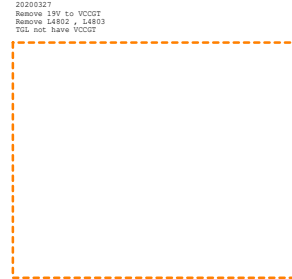
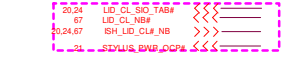
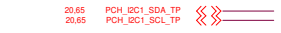
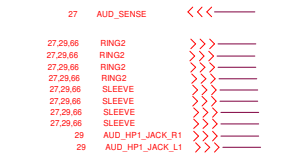
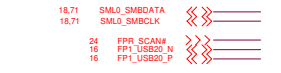
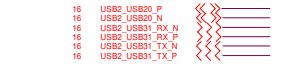
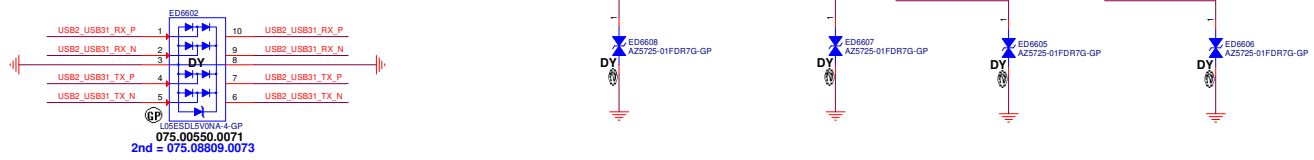
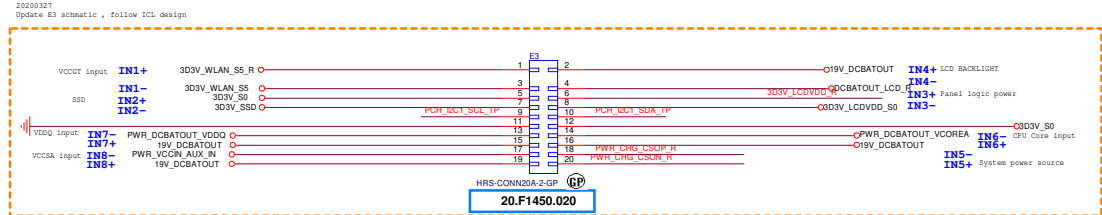


Table 1. Current Limit RSET Value for G517AH

RSET(Ω)	Current Limit Min (A)	Current Limit Typ (A)	Current Limit Max (A)
2.58	2.49	2.7	2.97
4.55	2.58	2.7	2.97
10.5	1.0	1.0	1.0
11.5	1.0	1.0	1.0
12.5	1.0	1.0	1.0
13.5	1.0	1.0	1.0
14.5	1.0	1.0	1.0
15.5	1.0	1.0	1.0
16.5	1.0	1.0	1.0
17.5	1.0	1.0	1.0
18.5	1.0	1.0	1.0
19.5	1.0	1.0	1.0
20.5	1.0	1.0	1.0
21.5	1.0	1.0	1.0
22.5	1.0	1.0	1.0
23.5	1.0	1.0	1.0
24.5	1.0	1.0	1.0
25.5	1.0	1.0	1.0
26.5	1.0	1.0	1.0
27.5	1.0	1.0	1.0
28.5	1.0	1.0	1.0
29.5	1.0	1.0	1.0
30.5	1.0	1.0	1.0
31.5	1.0	1.0	1.0
32.5	1.0	1.0	1.0
33.5	1.0	1.0	1.0
34.5	1.0	1.0	1.0
35.5	1.0	1.0	1.0
36.5	1.0	1.0	1.0
37.5	1.0	1.0	1.0
38.5	1.0	1.0	1.0
39.5	1.0	1.0	1.0
40.5	1.0	1.0	1.0
41.5	1.0	1.0	1.0
42.5	1.0	1.0	1.0
43.5	1.0	1.0	1.0
44.5	1.0	1.0	1.0
45.5	1.0	1.0	1.0
46.5	1.0	1.0	1.0
47.5	1.0	1.0	1.0
48.5	1.0	1.0	1.0
49.5	1.0	1.0	1.0
50.5	1.0	1.0	1.0
51.5	1.0	1.0	1.0
52.5	1.0	1.0	1.0
53.5	1.0	1.0	1.0
54.5	1.0	1.0	1.0
55.5	1.0	1.0	1.0
56.5	1.0	1.0	1.0
57.5	1.0	1.0	1.0
58.5	1.0	1.0	1.0
59.5	1.0	1.0	1.0
60.5	1.0	1.0	1.0
61.5	1.0	1.0	1.0
62.5	1.0	1.0	1.0
63.5	1.0	1.0	1.0
64.5	1.0	1.0	1.0
65.5	1.0	1.0	1.0



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File: **IO Board Connector**

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20,24,66 ISH_LID_CL#_NB > > _____



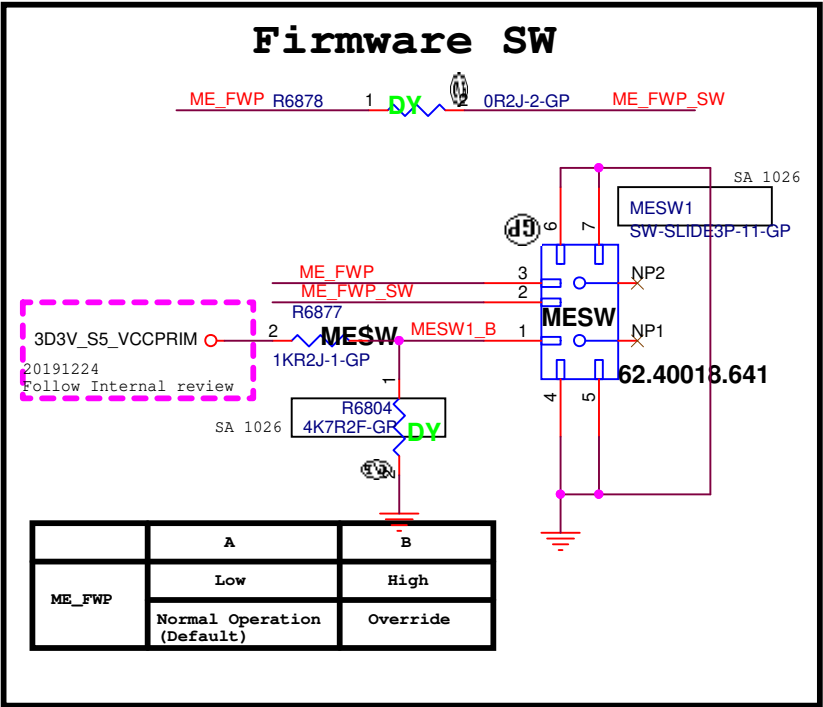
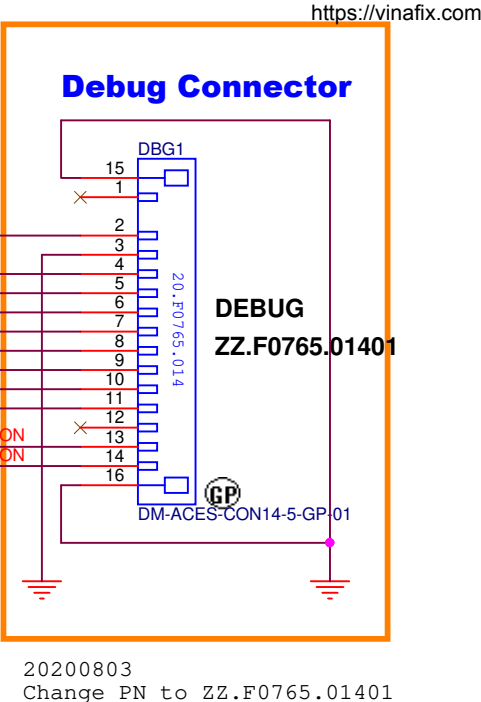
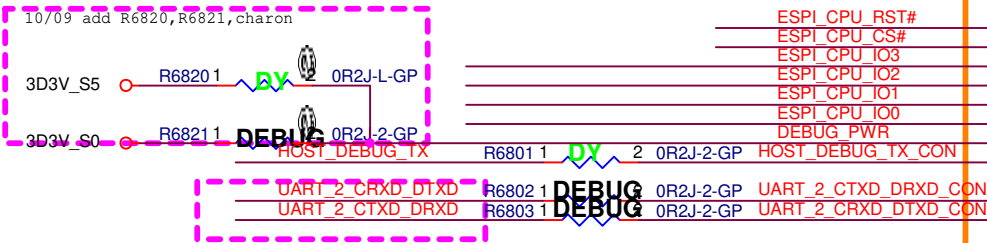
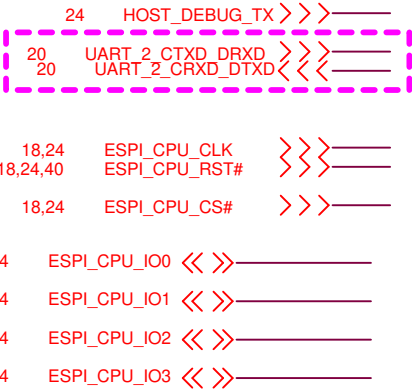
Lid Wake

Hellcat 15" Upsell TGL


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-1

105

Main Func = Debug



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Title

Dubug connector

Size A4

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Main FUNC = GMR

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Move to IO Board




```

24      UPD1_SMBCLK      >>>
24      UPD1_SMBDAT     >>>
24      CGO2_SC_INT#    >>>
74      PD_VBUS_C_CTRL1 >>>

73      USB1_CON_CC1     <<<
73      USB1_CON_CC2     <<<
146     PROCHOT_N_CPU    <<<
       VBUS_C_CTRL_P3_GPO <<<
17,72   TBT_PD_ALERT#   >>>

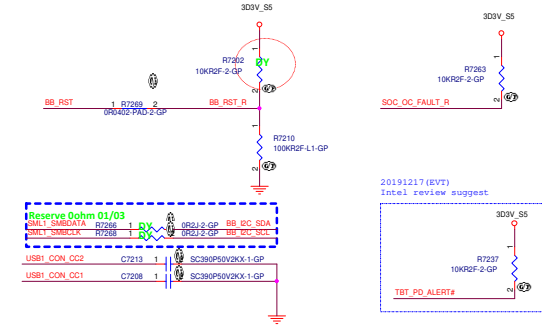
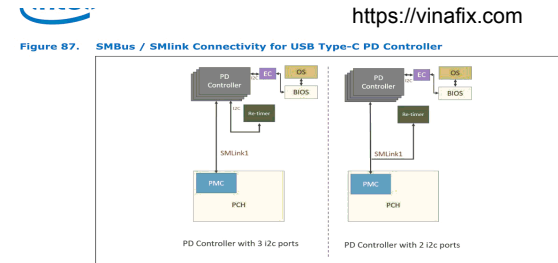
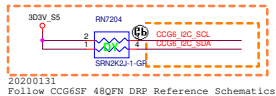
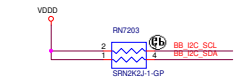
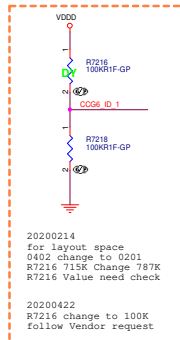
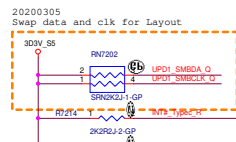
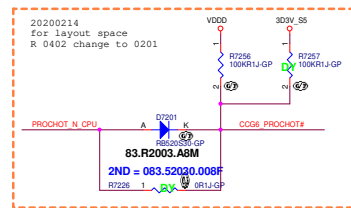
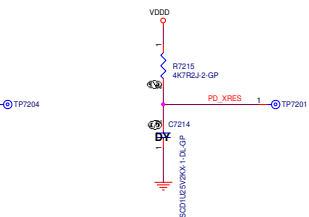
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16      USB1_USBD20_N    >>>
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       USB1_USBD20_CMCT_N >>>
       USB1_USBD20_CMIOB_N >>>
       USB1_CON_SBU1     >>>
       USB1_CON_SBU2     >>>

       USB1_BB_SBU1      >>>
       USB1_BB_SBU2      >>>
       SOC_OC_FAULT_R    >>>
       BB_RST            >>>
       TBT_PD_ALERT#     >>>

18      SML1_SMBCLK     >>>
18      SML1_SMBDATA    >>>

73      RETIMER_PWREN   >>>
16,71   TBT_FORCE_PWR   >>>

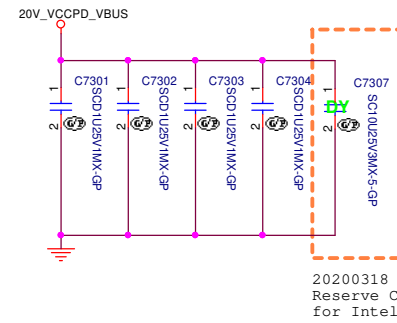
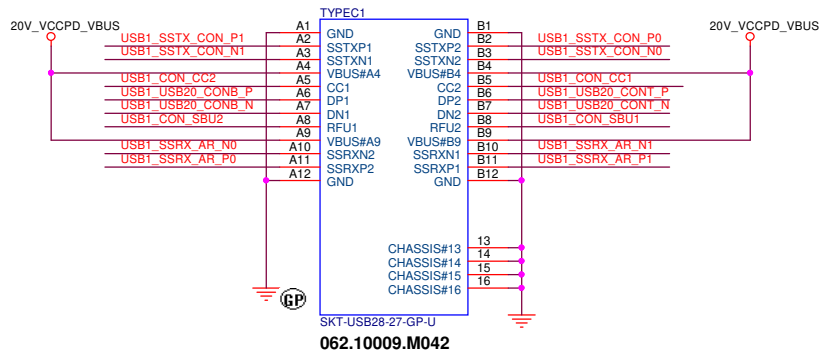
```



	Dell TGL Platform MOD_ID Options		
MUX	MOD_ID1	MOD_ID2	Description
BB8040R	L0	N/A	TBT Configuration w/BB Retimer
BB8010R	L2	N/A	non-TBT Configuration w/BB Retimer
TUSB545/1046	L6	L0	TUSB546 Equalizer config #1
TUSB545/1046	L6	L1 - L3	Reserved for TUSB546 Equalizer config #2,3,4 reserved

Main Func = TypeC

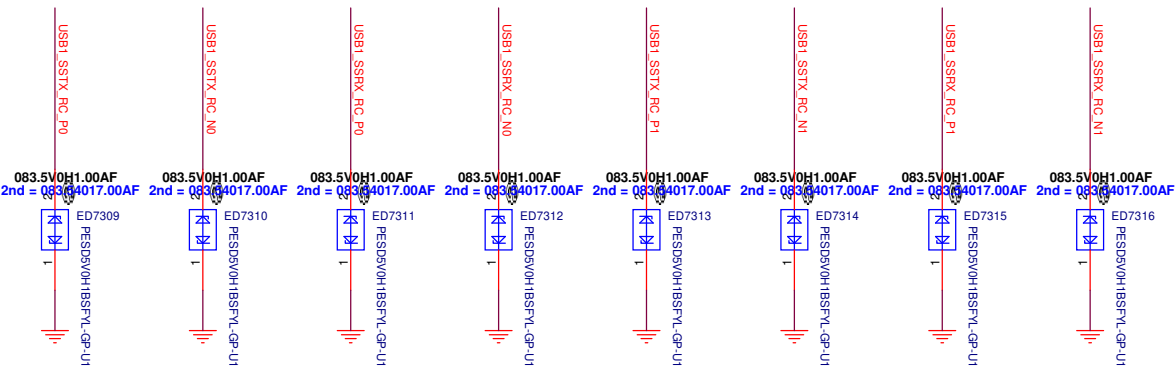
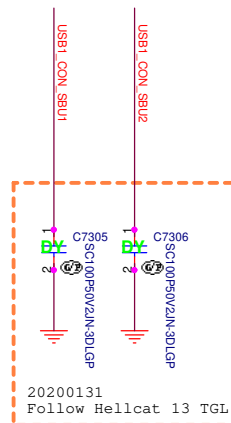
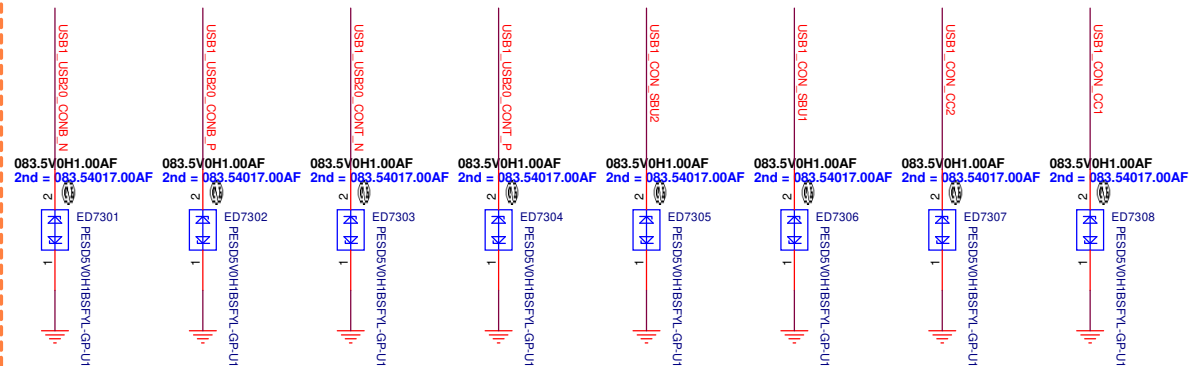
USB1



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20200213
Change Part
Only 083.5V0H1.00AF Can passed ESD protection for USB3.1 Gen2.



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EXT IO (Thunderbolt(3/3)/Type C Conn)

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Main FUNC = LPS

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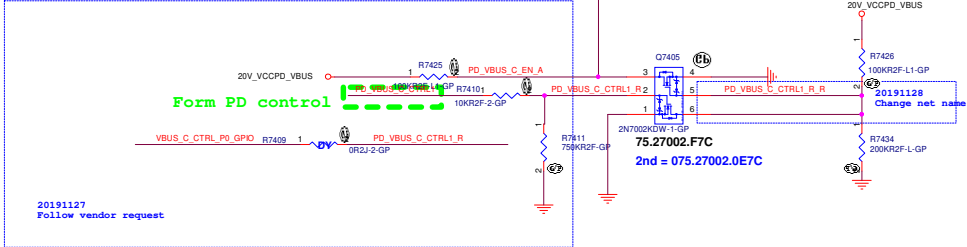
72 PD_VBUS_C_CTRL1 >>>_____

72 VBUS_C_CTRL_P0_GPIO <<<—

24 TYPEC_DCIN1_EN# >>>_____

```
44  VCCPD_VBUS_ACK  >>>_____
```


Default: High
Active : Low
R013 Shauchi



Form PD control

(Blanking)

<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

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Main Func = dGPU

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16 GFX_PCIE_RX_P0 <<<<=====
16 GFX_PCIE_RX_N0 >>>>=====
16 GFX_PCIE_TX_P0 >>>>=====
16 GFX_PCIE_TX_N0 <<<<=====
16 GFX_PCIE_RX_P1 <<<<=====
16 GFX_PCIE_RX_N1 >>>>=====
16 GFX_PCIE_TX_P1 >>>>=====
16 GFX_PCIE_TX_N1 <<<<=====
16 GFX_PCIE_RX_P2 <<<<=====
16 GFX_PCIE_RX_N2 >>>>=====
16 GFX_PCIE_TX_P2 >>>>=====
16 GFX_PCIE_TX_N2 <<<<=====
16 GFX_PCIE_RX_P3 <<<<=====
16 GFX_PCIE_RX_N3 >>>>=====
16 GFX_PCIE_TX_P3 >>>>=====
16 GFX_PCIE_TX_N3 <<<<=====

18 GFX_CLK_CPU_P >>>>=====
18 GFX_CLK_CPU_N >>>>=====

20 GPU_WAKE# >>>>=====

80,85,88 PWR_VGA_READY >>>>=====

8 24,77,88 RTD3_COLD_MOD# >>>>=====

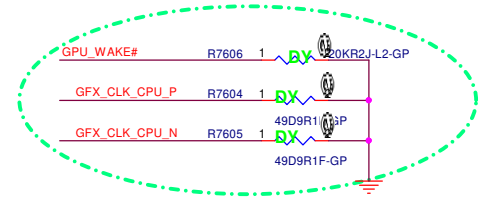
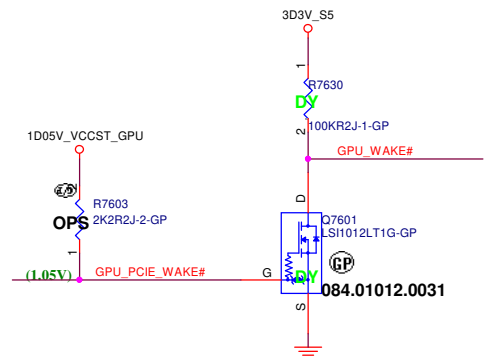
88 SYS_PEX_RST_MON# >>>>=====

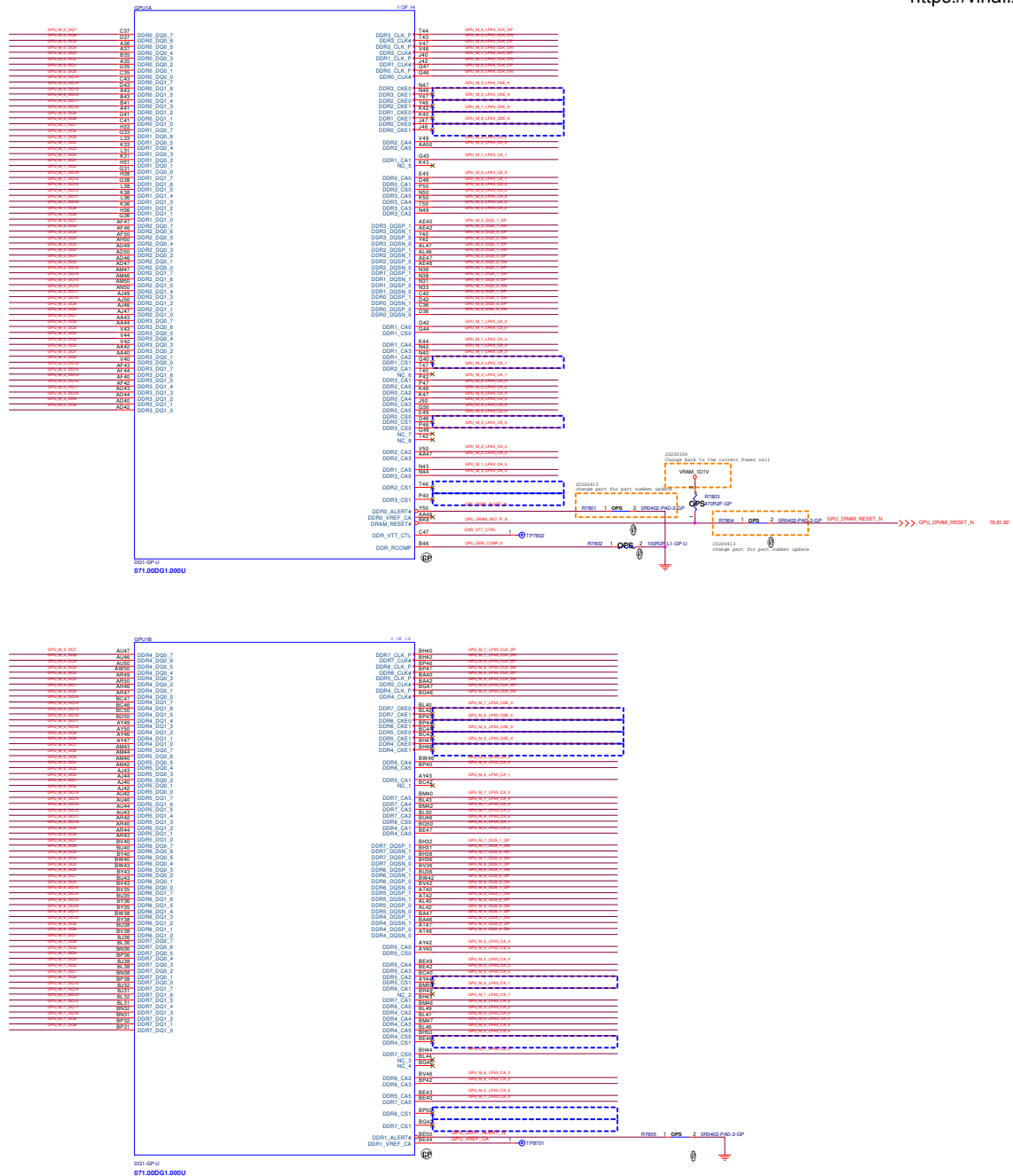
GFX_PCIE_RX_P0 C7601 1 OPS2 SCD22U10V1KX-1-GP GFX_PCIE_RX_CON_P0 BP17
GFX_PCIE_RX_N0 C7602 1 OPS2 SCD22U10V1KX-1-GP GFX_PCIE_RX_CON_N0 BT17
GFX_PCIE_RX_P1 C7603 1 OPS2 SCD22U10V1KX-1-GP GFX_PCIE_RX_CON_P1 BT19
GFX_PCIE_RX_N1 C7604 1 OPS2 SCD22U10V1KX-1-GP GFX_PCIE_RX_CON_N1 BU19
GFX_PCIE_RX_P2 C7605 1 OPS2 SCD22U10V1KX-1-GP GFX_PCIE_RX_CON_P2 BP20
GFX_PCIE_RX_N2 C7606 1 OPS2 SCD22U10V1KX-1-GP GFX_PCIE_RX_CON_N2 BT20
GFX_PCIE_RX_P3 C7607 1 OPS2 SCD22U10V1KX-1-GP GFX_PCIE_RX_CON_P3 BT22
GFX_PCIE_RX_N3 C7608 1 OPS2 SCD22U10V1KX-1-GP GFX_PCIE_RX_CON_N3 BU22

GPU1C 3 OF 14
PCIBCLK_P BY14 GFX_CLK_CPU_P
PCIBCLK_N BW14 GFX_CLK_CPU_N
PERST# BJ12 SYS_PEX_RST_MON#
WAKE# BV6 GPU_PCIE_WAKE#
PCIE_RCOMP_P BY32 GPU_PCIE4_RCOMP_P
PCIE_RCOMP_N BW32 GPU_PCIE4_RCOMP_N
RSVD_TP_1 BJ25 GPU_PCIE_DFX_DAMON_OBS_DP
RSVD_TP_2 BJ27 GPU_PCIE_DFX_DAMON_OBS_DN
PCIE_RX_P_0 BW17 PCIE_RX_P_0
PCIE_RX_N_0 BY17 PCIE_RX_N_0
PCIE_RX_P_1 BW19 PCIE_RX_P_1
PCIE_RX_N_1 BY19 PCIE_RX_N_1
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PCIE_RX_N_2 BY20 PCIE_RX_N_2
PCIE_RX_P_3 BW22 PCIE_RX_P_3
PCIE_RX_N_3 BY22 PCIE_RX_N_3
PCIE_RX_P_4 BY24 PCIE_RX_P_4
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PCIE_RX_N_6 BW27 PCIE_RX_N_6
PCIE_RX_P_7 BY29 PCIE_RX_P_7
PCIE_RX_N_7 BW29 PCIE_RX_N_7
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PCIE_TX_N_0 BT17 PCIE_TX_N_0
PCIE_TX_P_1 BT19 PCIE_TX_P_1
PCIE_TX_N_1 BU19 PCIE_TX_N_1
PCIE_TX_P_2 BP20 PCIE_TX_P_2
PCIE_TX_N_2 BT20 PCIE_TX_N_2
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PCIE_TX_N_3 BU22 PCIE_TX_N_3
PCIE_TX_P_4 BP24 PCIE_TX_P_4
PCIE_TX_N_4 BT24 PCIE_TX_N_4
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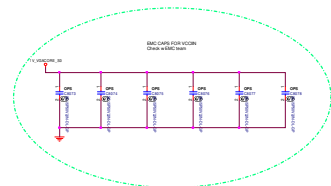
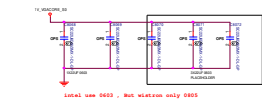
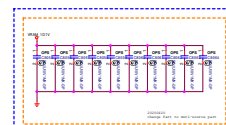
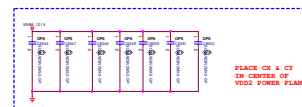
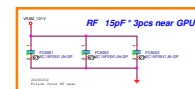
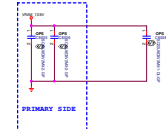
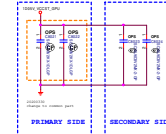
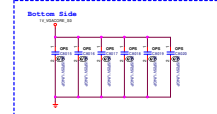
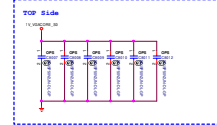
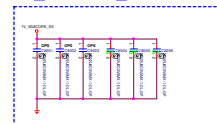
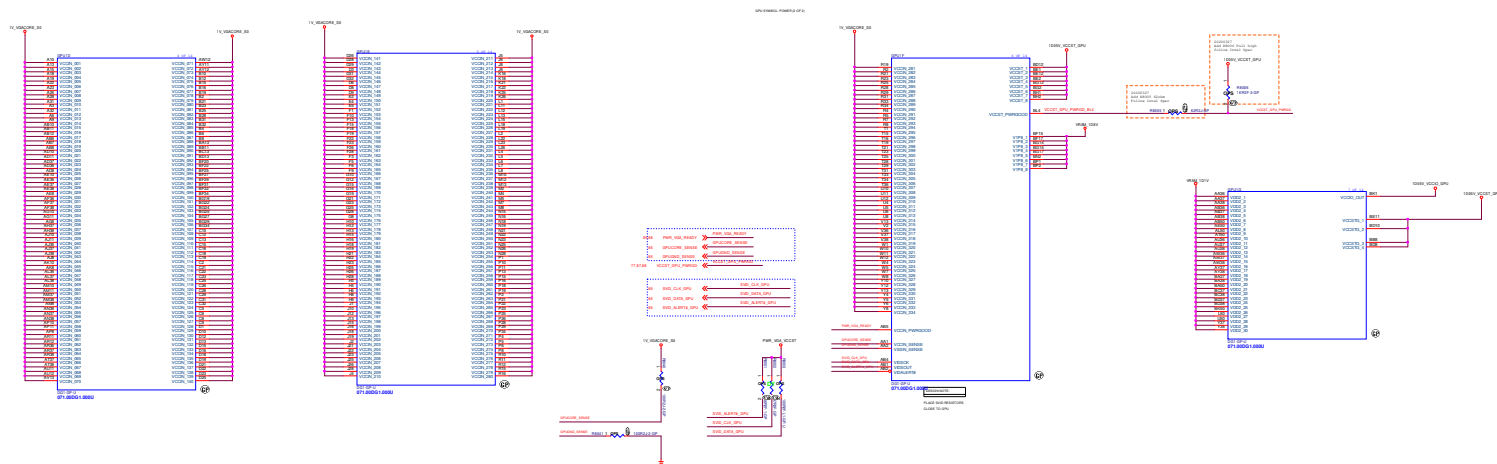
DG1-GP-U
071.00DG1.000U

20191231
Remove R3075700 internal modify





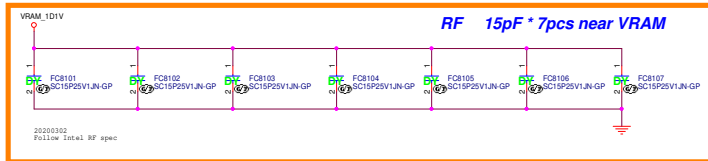
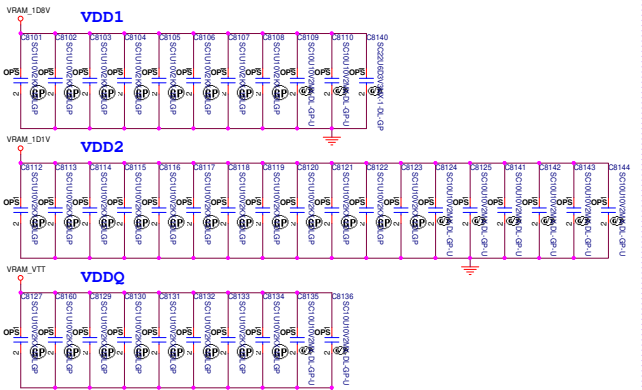
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For 4PCS RAM place

Memory Configuration	Power Domain	Decoupling Location	Qty x μ F (size)
LPDDR4X x32 Decoupling Config-1	VDD2	6 caps per Dram, 2 per long edge, 1 per short edge evenly distribute among all Drams	24x 1 μ F (0402)
	VDDQ	4 per Dram, 2 per corner (each Dram Package has 4 pairs of VDD1 BGAs, each pair gets 1 cap) evenly distribute among all Drams	5x 10 μ F (0603)
	VDD1	4 per Dram, 1 per corner (each Dram Package has 4 pairs of VDD1 BGAs, each pair gets 1 cap) evenly distribute	16x 1 μ F (0402) 5x 10 μ F (0603)

Layout Note:Place as pic..



	LPDDR4		LPDDR4X	
VDDQ	1.1V	410mA	0.6V	185mA
VDD1	1.8V	6.8mA	1.8V	12mA
VDD2	1.1V	290mA	1.1V	465mA

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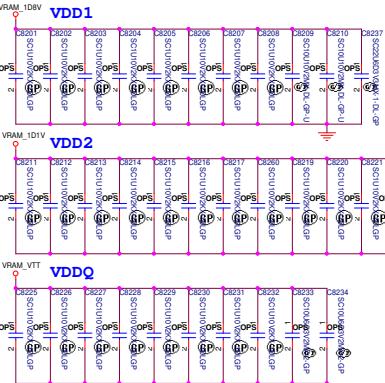
GPU-VRAM1.2 (1/4)

Size: 11mm x 11mm x 1.2mm
Document Number: Helicat 15" Upsell TGL
Date: Monday, August 05, 2020
Sheet: 81 of 108

For 4PCS RAM place

Memory Configuration	Power Domain	Decoupling Location	Qty x μ F (size)
LPDDR4X x32 Decoupling Config-1	VDD2	6 caps per Dram, 2 per long edge, 1 per short edge evenly distribute among all Drams	24x 1 μ F (0402)
	VDDQ	4 per Dram, 2 per corner (each Dram Package has 4 pairs of VDD1 BGAs, each pair gets 1 cap) evenly distribute among all Drams	16x 1 μ F (0402)
	VDD1	4 per Dram, 1 per corner (each Dram Package has 4 pairs of VDD1 BGAs, each pair gets 1 cap) evenly distribute	5x 10 μ F (0603)
			16x 1 μ F (0402)

Layout Note:Place as pic..



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Helicat 15" Upsell TGL

Rev

-1

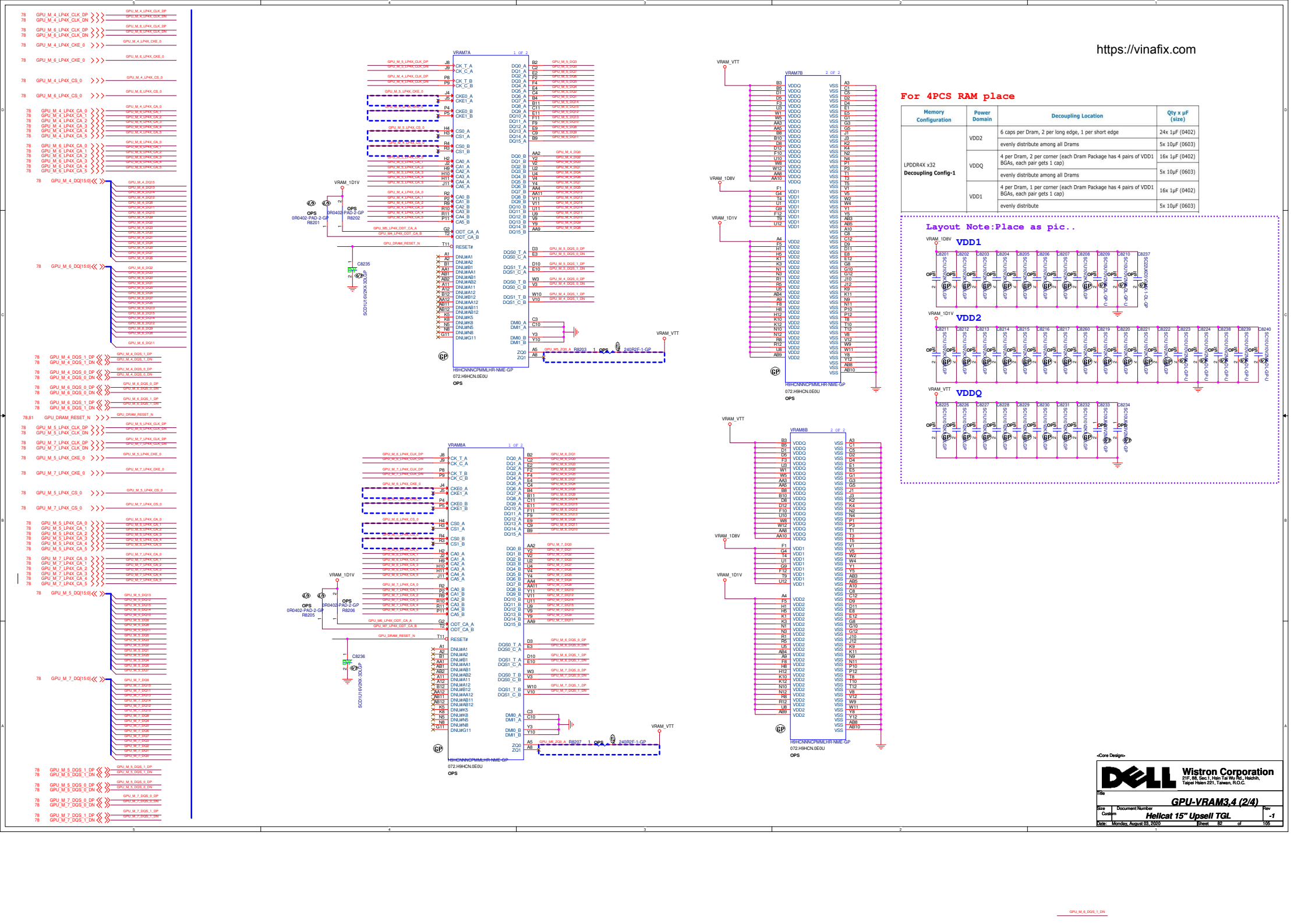
Date: Monday, August 05, 2020

Sheet


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105



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Title			
GPU-VRAM5,6 (3/4)			
Size	Document Number		Rev
A3	Hellcat 15" Upsell TGL		-1
Date:	Monday, August 03, 2020		Sheet 83 of 105

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Taipei Hsien 221, Taiwan, R.O.C.

Title

GPU-VRAM7,8 (4/4)

Size

A3

Document Number

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Rev

-1

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SVID

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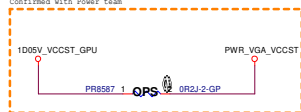
80 SVID_DATA_GPU >> SVID_DATA_GPU
80 SVID_ALERT#_GPU >> SVID_ALERT#_GPU

```

77 PWR_VGA_PROCHOT_N << PWR_VGA_PROCHOT_N

80	GPUCORE_SENSE	>>	GPUCORE_SENSE
80	GPUGND_SENSE	>>	GPUGND_SENSE

20200701
 ID05V_VCCST modify to ID05V_VCCST_GPU
 follow Intel TGL DGI TDK
 Continued with Bruce team

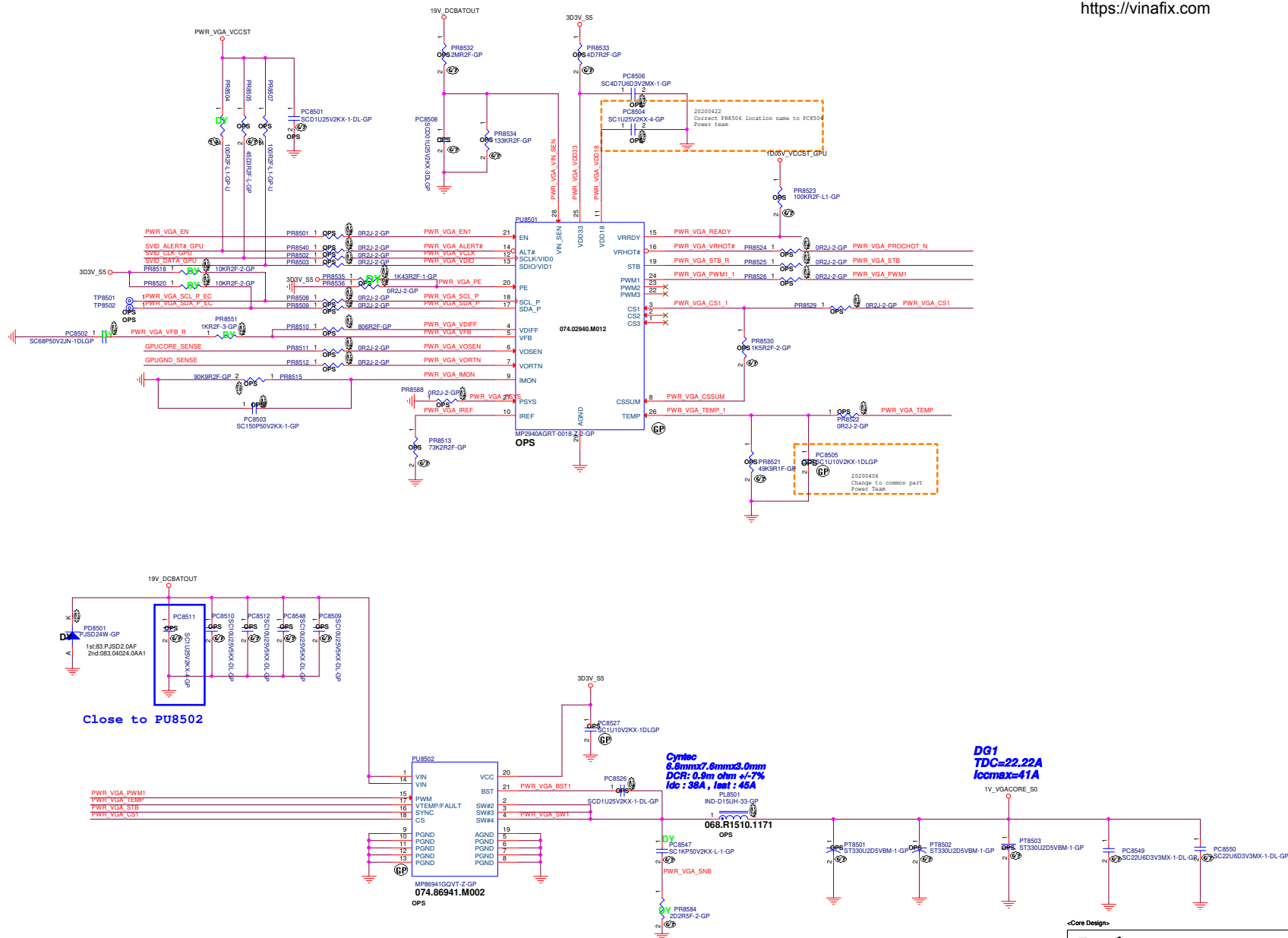


19V_DCBATOUT

TC8501
ST33U25VDM-5-GP

077.23361.0001
2nd = 077.53361.0021

20200514
Change to DY
Follow internal review



<Core Design:



Title			
POWER (MP2940A VGA)			
Size	Document Number	Rev	
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Main Func = dGPU

OFFPAGE

S5(PM_SLP_S4#)

17,40,66 SIO_SLP_S4#

S3(VTT_CNTL)

18,77,87,88 RTD3_COLD_POR#

PH on EE Side

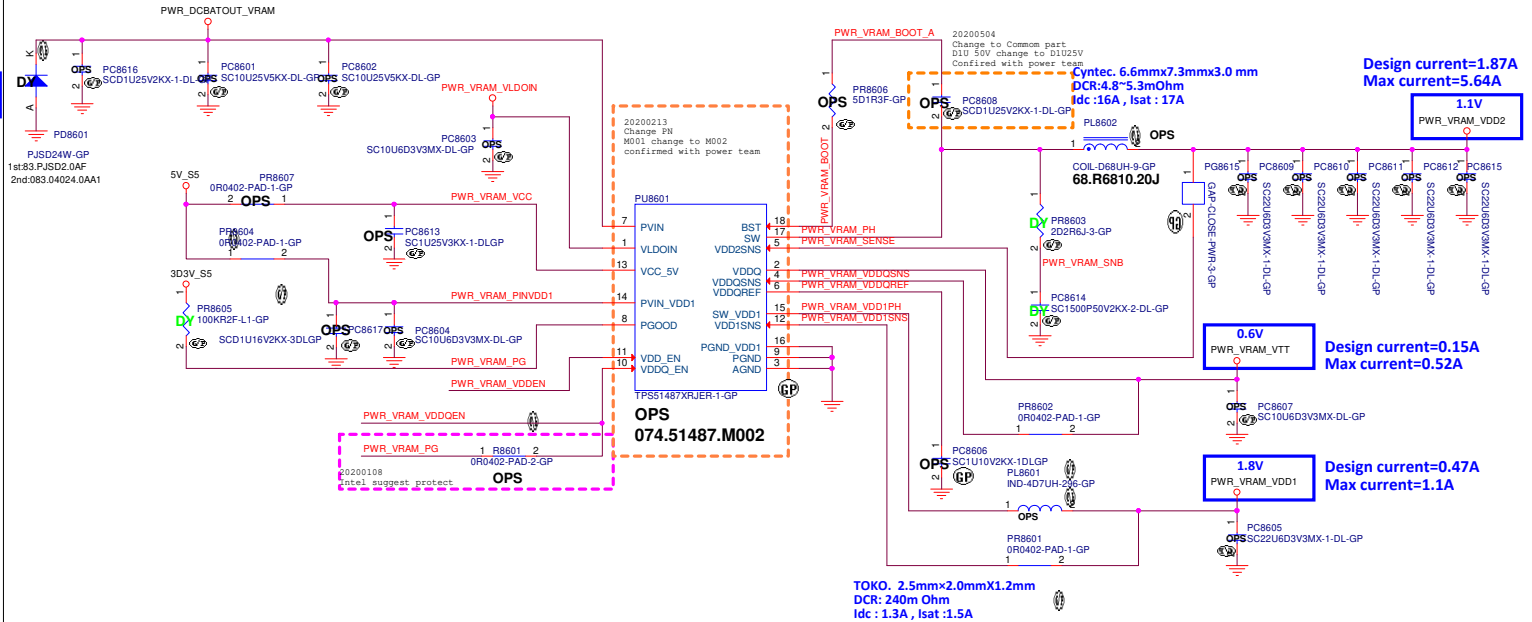
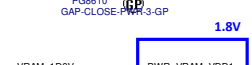
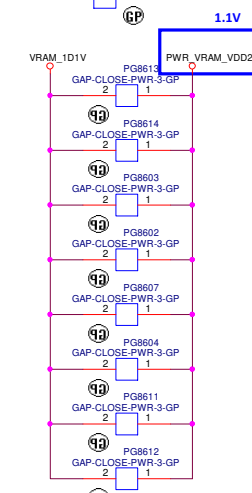
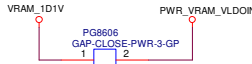
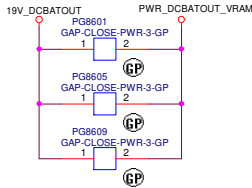
PWR_VRAM_PG

VCCST_GPU_PWRGQX <<< VCCST_GPU_PWRGD

88 PWR_VRAM_VDDEN <<<

88 PWR_VRAM_VDDQEN <<<

OFFPAGE_GAP



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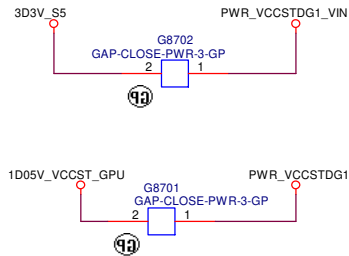
<Core Design>

DELL		Wistron Corporation	
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Title POWER (TPS51487X_VDDQ)			
Size	Document Number	Rev	
Custom	Helicat 15" Upsell TGL	-1	
Date: Monday, August 03, 2020	Sheet 86	of	105

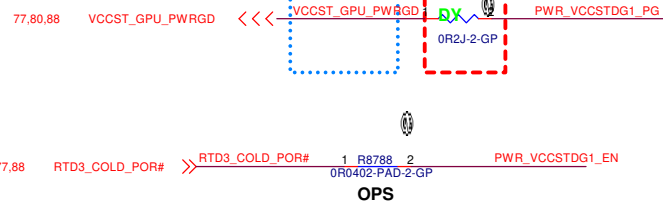
Main Func = VCCSTDG1

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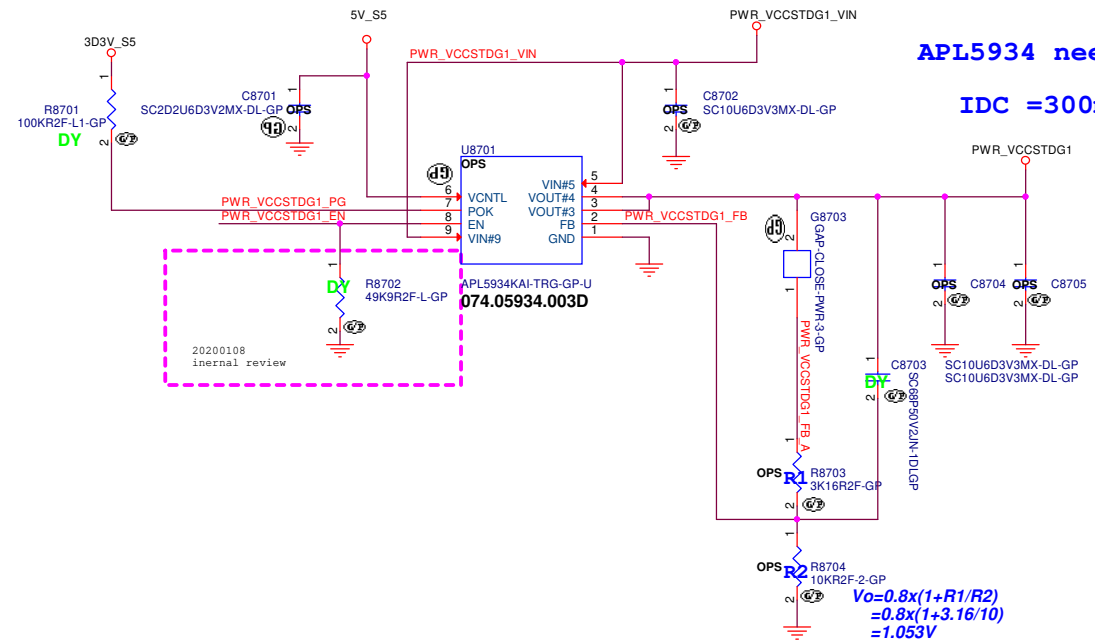
OFFPAGE_GAP



PH on EE Side



APL5934 for VCCSTDG1



APL5934 need <1.8W

IDC =300mA

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Title POWER (1D05V_VCCST_GPU)		
Size A3	Document Number Hellicat 15" Upsell TGL	Rev -1
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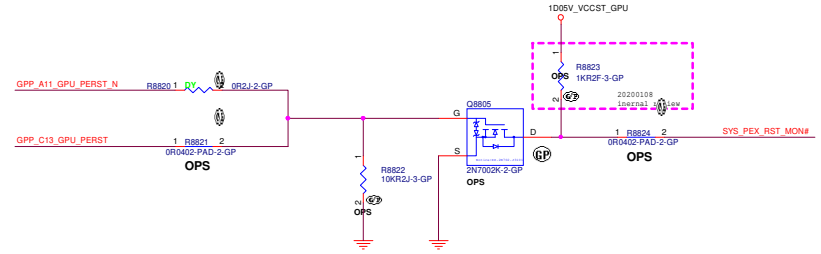
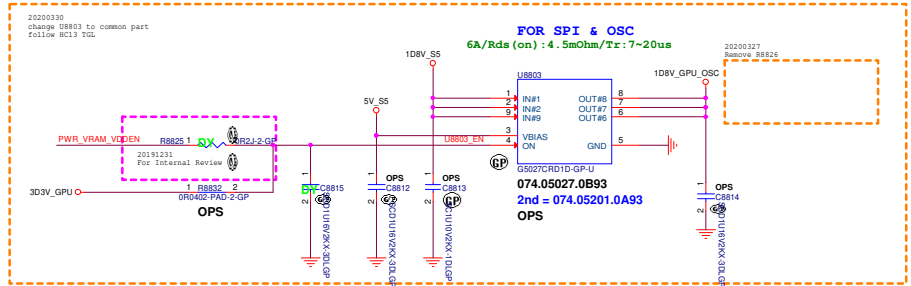
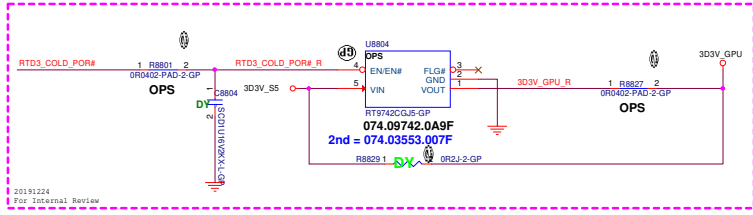
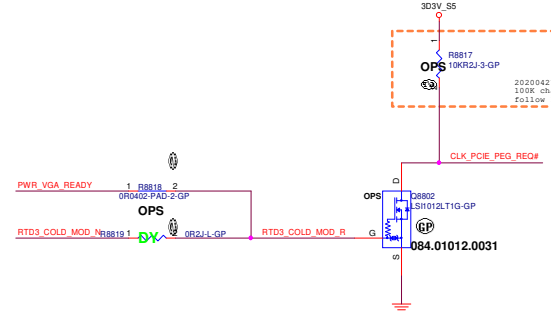
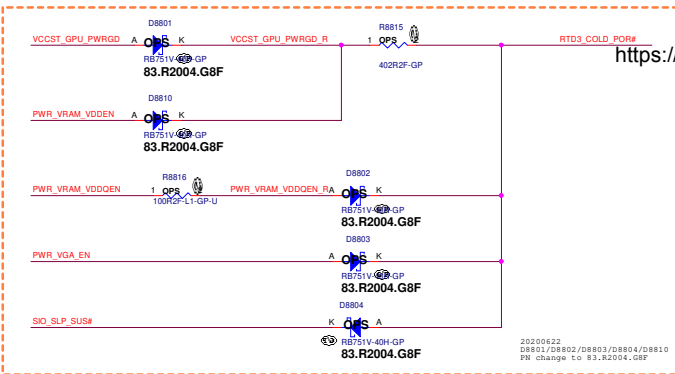
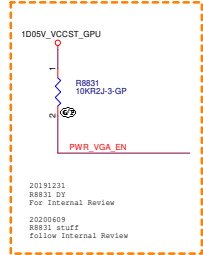
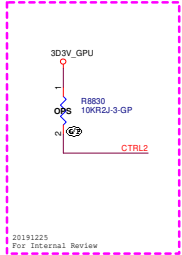
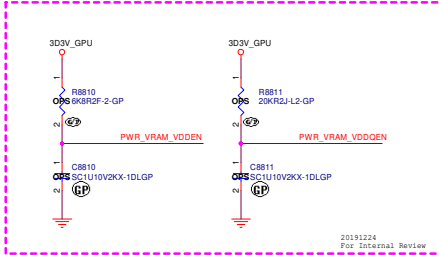
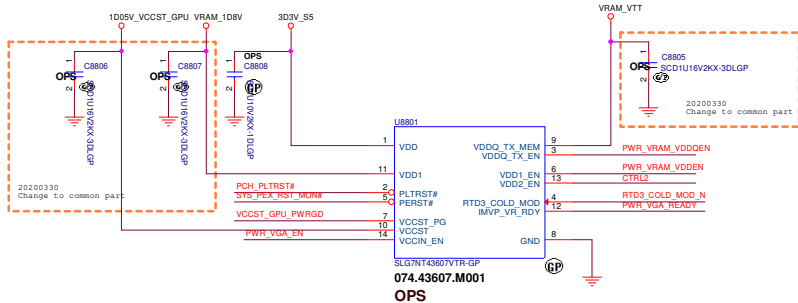
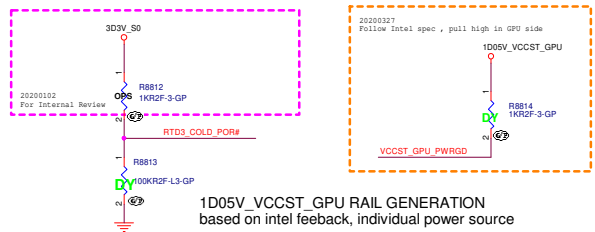
Main Func = dGPU

18,24,77 RTD3_COLD_MOD_N <<< _____
18,77,87 RTD3_COLD_POR# <<< _____
17,40,61,88 SID_SLP_SUS# <<< _____

85 PWR_VGA_EN >>> PWR_VGA_EN
77,80,87 VCCST_GPU_PWRGD <<< VCCST_GPU_PWRGD

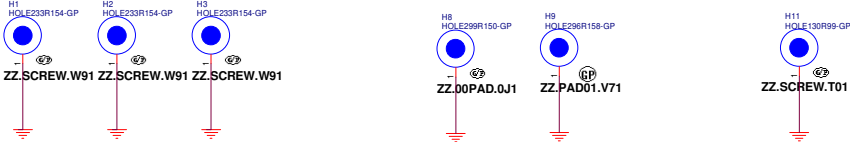
18 CLK_PCIE_PEG_REQ# <<< _____
80,85 PWR_VGA_READY >>> PWR_VGA_READY
76 SYS_PEX_RST_MON# >>> _____
17,26,61,63,66,71 PCH_PLTRST# >>> _____
17,40,61,88 SID_SLP_SUS# <<< _____
86 PWR_VRAM_VDDEN <<< PWR_VRAM_VDDEN

19 GPP_A11_GPU_PERST_N >>> _____
20 GPP_C13_GPU_PERST >>> _____
86 PWR_VRAM_VDDQEN <<< PWR_VRAM_VDDQEN

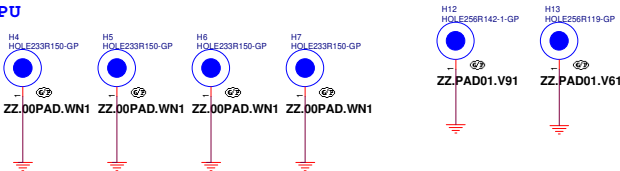


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GPU



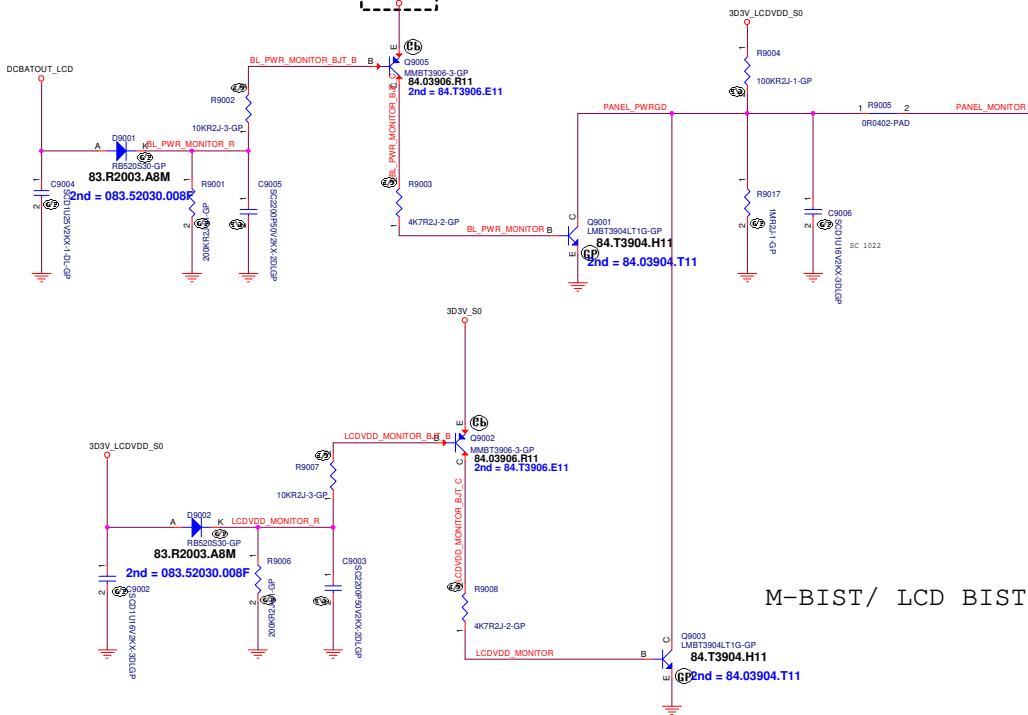
CPU



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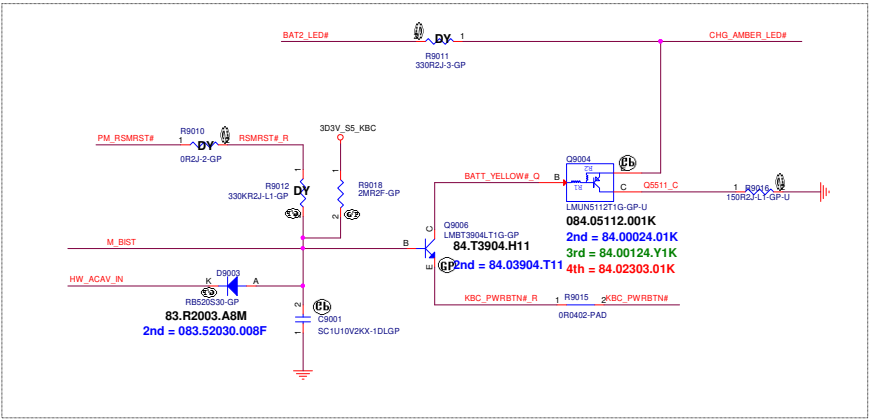
LCD BIST for G10 (Was test only for G9)

- 24,64,90 CHG_AMBER_LED# >>>
- 24 BAT2_LED# >>>
- 24,66 KBC_PWRBTN# <<<
- 17 PM_RSMRST# <<<
- 24,44 HW_ACAV_IN <<<
- 24 PANEL_MONITOR <<<
- 24 M_BIST <<<
- 24,64,90 CHG_AMBER_LED# <<<



M-BIST/ LCD BIST -1890201

M-BIST for G10 (Proposed schematic)



5

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B

B

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A

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Title					
INT IO (TPM)					
Size	Document Number				Rev
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4

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1

<Core Design>

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Title <i>Finger Print</i>			
Size A3	Document Number <i>Helicat 15" Upsell TGL</i>		Rev <i>-1</i>
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Title

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Size
A3

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Title

LVDS Switch

Size
A4

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Main Func = Firmware SW

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Title

CRT Switch

Size

A3

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Title			Debug(XDP/HDT)		
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Block Diagram

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DATE	VERSION	DATE	Page	Modify List												OWNER													



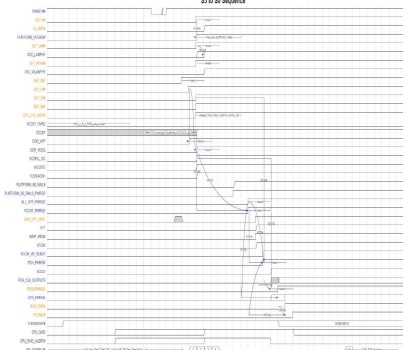
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Intel-Power Up Sequence



Tiger Lake-Y and U Timing Diagram for G3 to S0[Non-Deep Sx Platform]

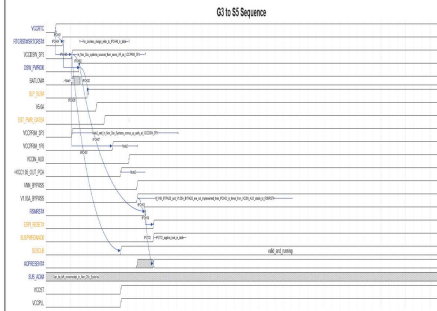
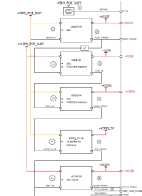
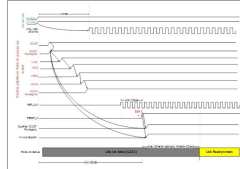
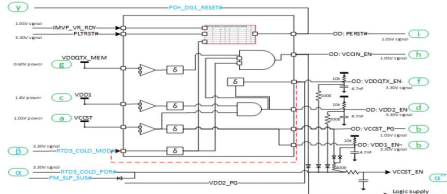
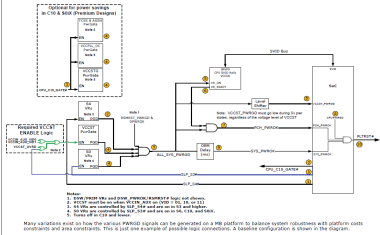
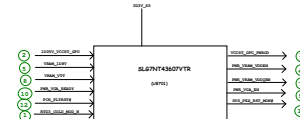
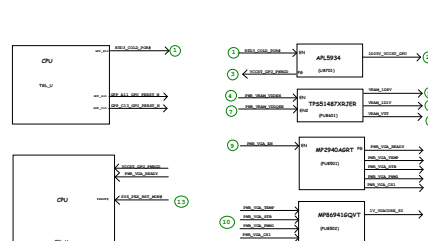
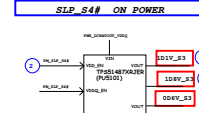
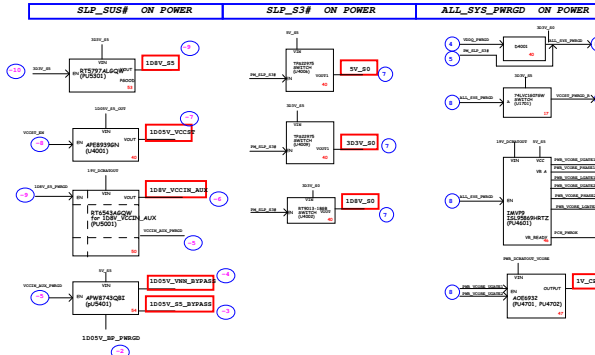
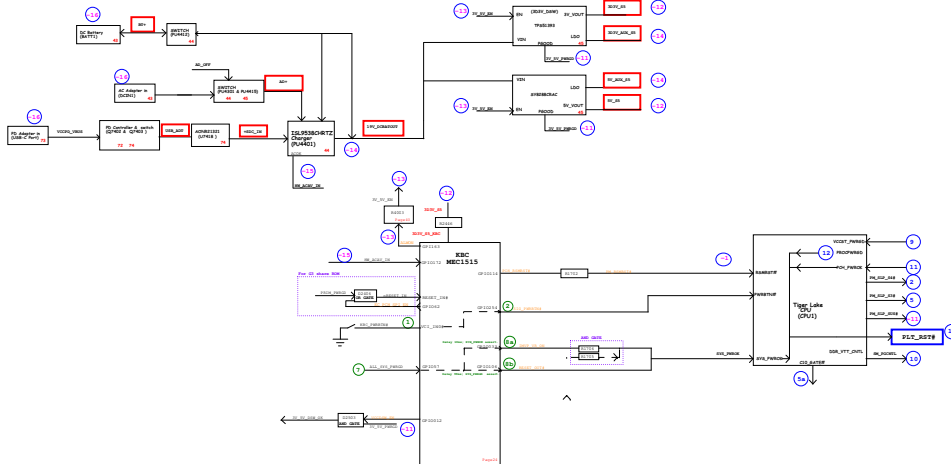
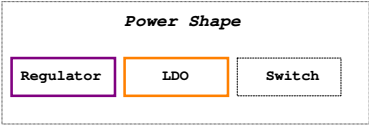
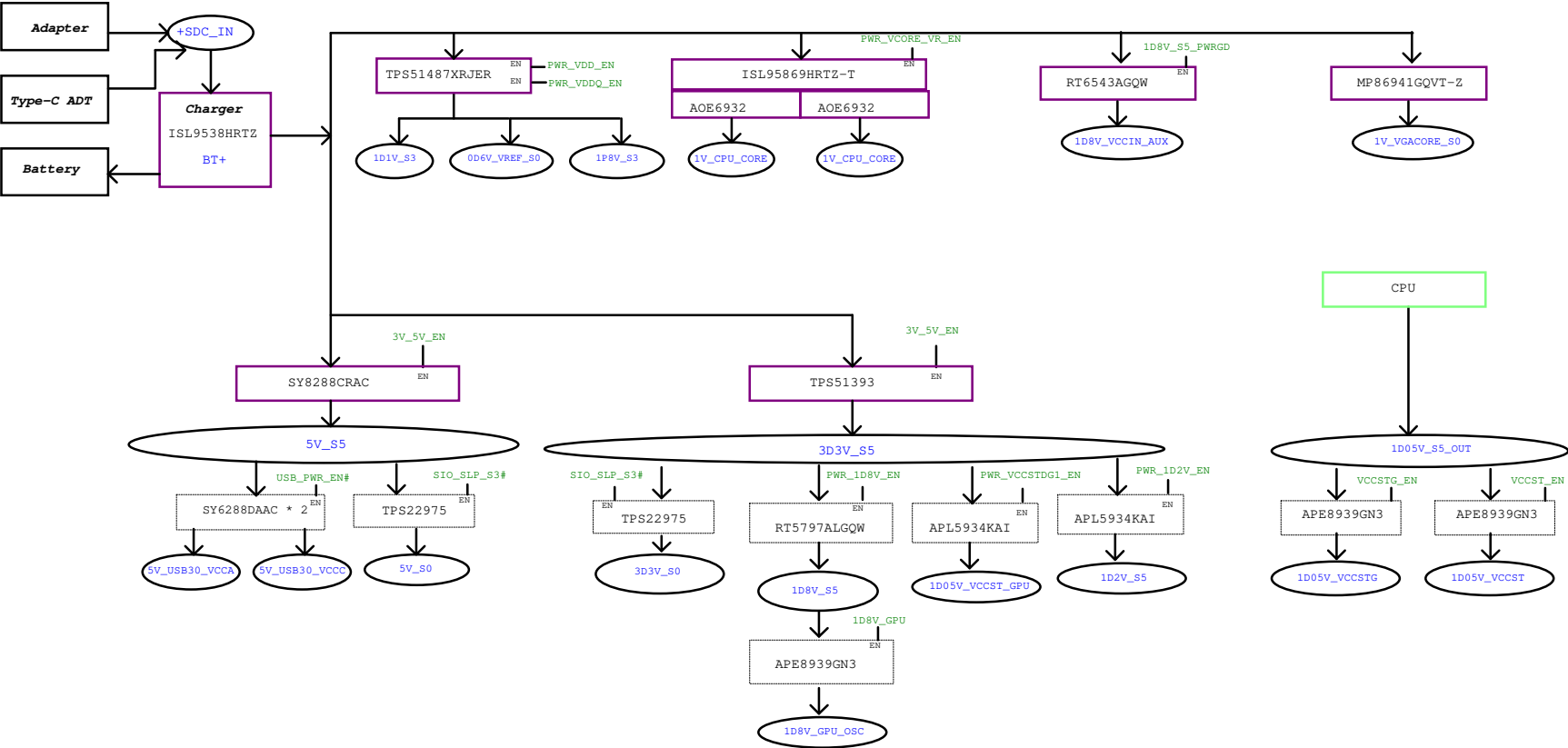


Figure 267. Tiger Lake Y and U (Premium) PWROK Generation Flow Diagram

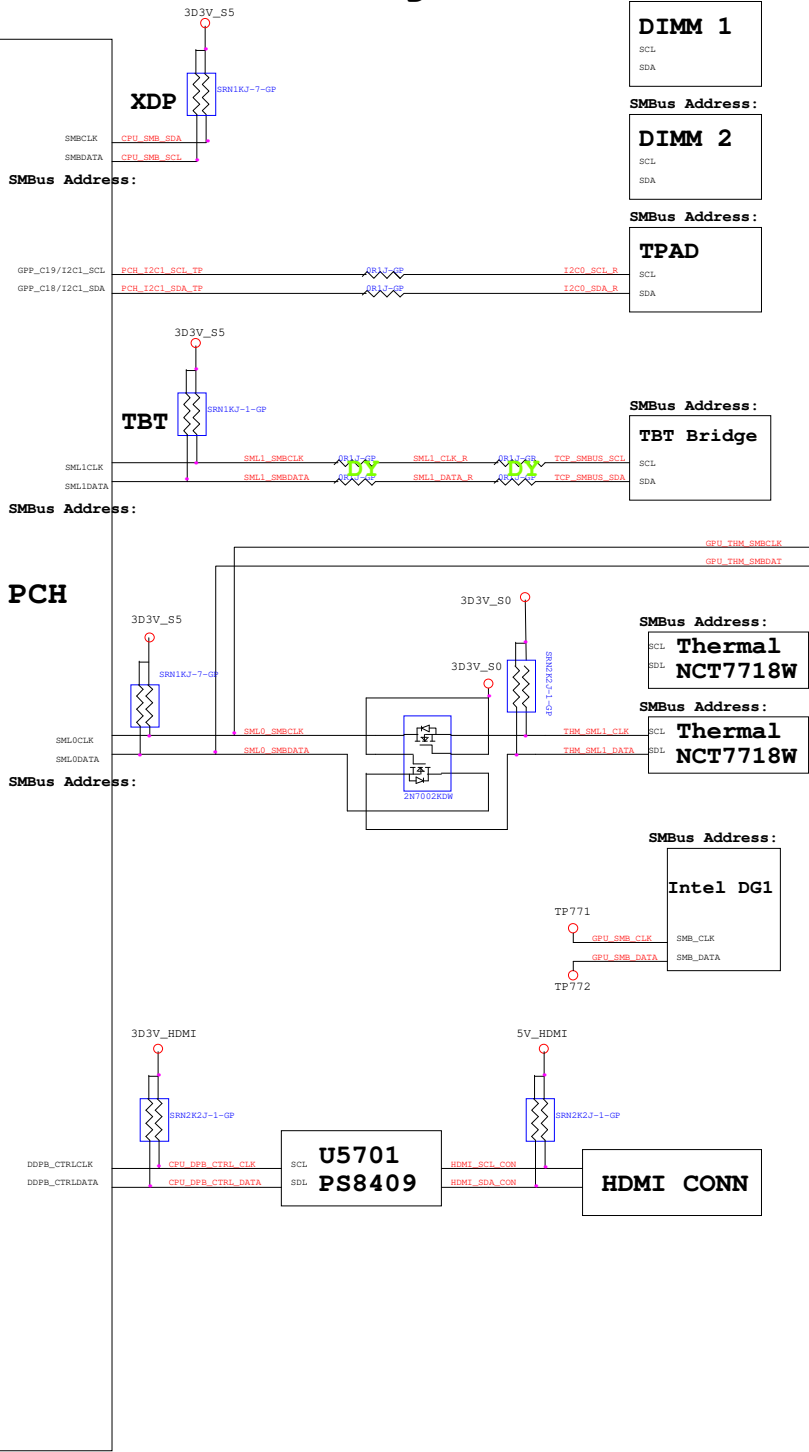


Tiger Lake U POWER UP SEQUENCE DIAGRAM



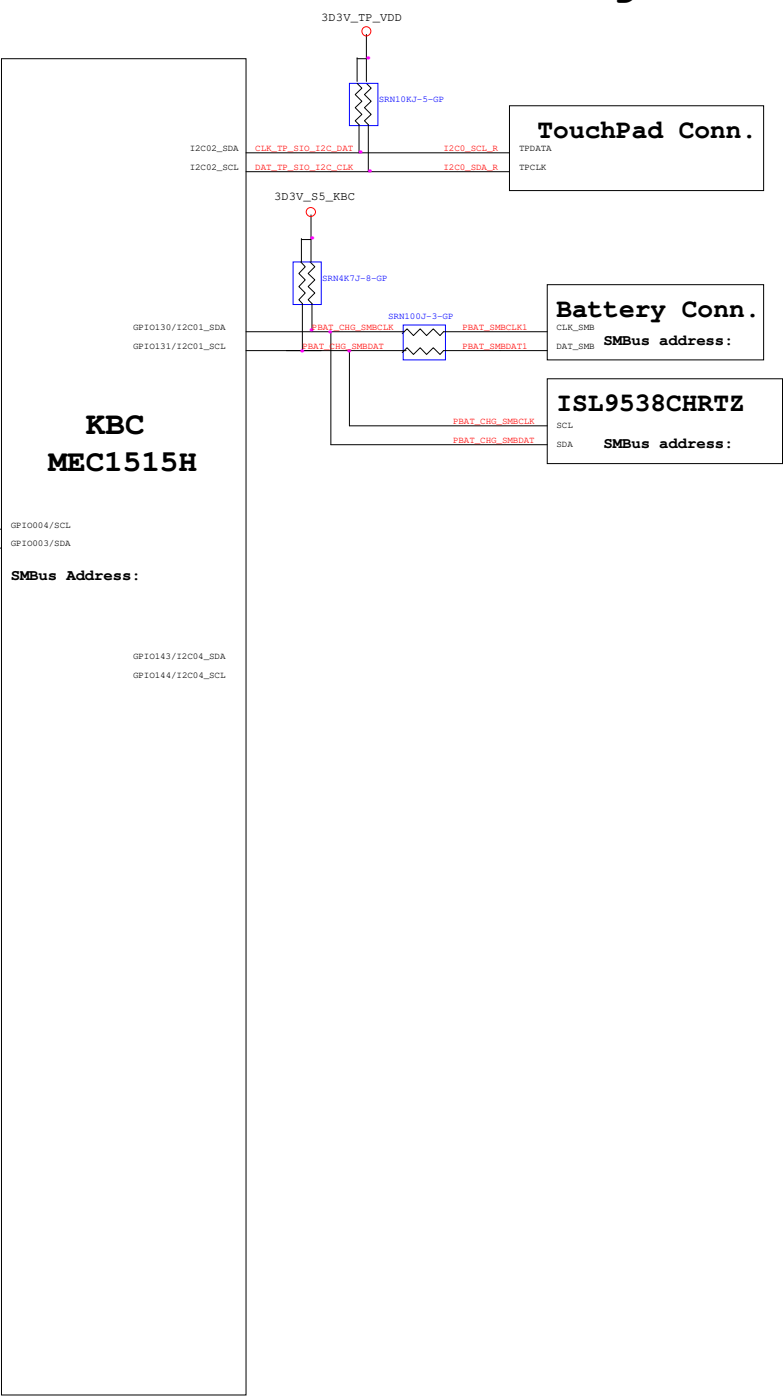


PCH SMBus Block Diagram

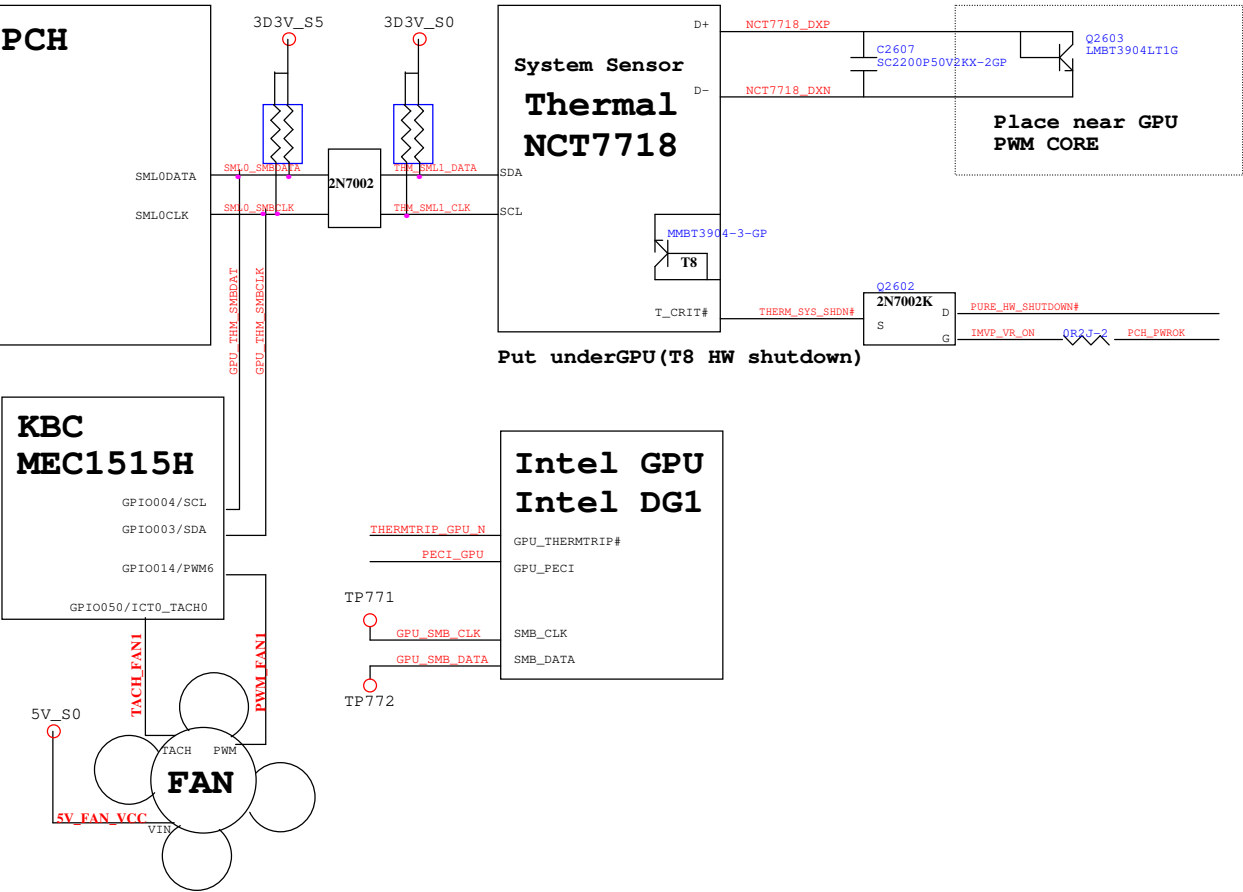


KBC SMBus Block Diagram

<https://vinafix.com>



Thermal Block Diagram



Audio Block Diagram

